A Portable High-Performance Fibre Channel Tester and Analyser*

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Abstract

This paper describes a high performance Fibre Channel (FC) tester and analyser that has been developed in a collaboration between CERN, RMKI and Hewlett-Packard/Geneva. The aim of this joint project was to build a portable and cheap Fibre Channel test box. Up to four test boxes can be controlled by a personal computer via a PCMCIA interface, making up a complex test system. This test system has several working modes: single and double line monitor, signal generator, N_Port emulator, fabric tester and fabric emulator. It can help the hardware and software development of N_Ports and F_Ports using correct and corrupted FC data bytes, data words, ordered sets, frames and protocols. It can also be used for testing upper level protocols, such as IP and SCSI. The tester can emulate different data sources for the development of FC equipment (data acquisition systems, event builders, etc.) used in high energy physics laboratories. It uses the 266 MBaud data transmission speed and can have electrical, LED and laser signal interfaces.

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1. Introduction

The Fibre Channel Standard (FCS) [1] defines a high-speed data transfer interface that can be used to connect together workstations, mainframes, supercomputers, storage devices and displays. The standard addresses the need for very fast transfers of large volumes of information and could relieve system manufacturers from the burden of supporting the variety of channels and networks currently in place, as it provides one standard for networking, storage and data transfer.

Fibre Channel (FC) ports can be connected as point-to-point links, in a loop or to a switch. The ports in a point-to-point connection are called N_Ports; if they can work in a loop they are called NL_Ports. An FC switch, or a network of switches, is called a fabric. The ports of it are called F_Ports.

Both optical and electrical media are supported, working from 133 Megabits/sec up to 1062 Megabits/sec, while distances up to 10 km are possible.

Information can flow between two ports in both directions simultaneously. Exchange is the name of the mechanism for coordinating the exchange of information between two N_Ports. The port starting the Exchange is called the Originator, the port that answers is called the Responder. The data is sent in frames that are maximum 2148 bytes long. Frames have a header and a checksum. A set of related frames for one operation is called a Sequence. For flow control the Fibre Channel standard uses a look-ahead, sliding-window scheme that also provides a guaranteed delivery capability. FCS has the ability to carry multiple existing protocols including IP and SCSI.

The advantages offered by Fibre Channel induced the manufacturers to develop FC components, systems and software. Developing FC ports necessitates the use of FC testers and analysers. This paper describes a recently developed tester produced in a collaboration of three institutions: CERN (European Laboratory for Particle Physics, Geneva, Switzerland), RMKI (Research Institute for Particle and Nuclear Physics, Budapest, Hungary) and HP/Geneva (Hewlett-Packard SA, Geneva, Switzerland).

The tester developed can be used to test FC ports and fabrics in different configurations. As it uses exchangeable link cards, ports with electrical and optical signal interfaces can be tested, with the limitation that only the 266 Megabits/sec link speed is supported. The tester can be used to test low level links, but as well to help software development, as it is capable of interpreting high-level protocols that are sent over the fibres. Furthermore, it has accurate timing facilities so latencies of fabrics and interfaces can be measured. For high energy physics laboratories, it can also be used to emulate different data sources for the development of FC equipment such as data acquisition systems and event builders.

The next section gives an overview of the tester's working modes. Section 3 and 4 detail the hardware and software architectures. A summary of present and future work is presented in section 5.

2. Working modes of the tester

The tester consists of one to four module cards. Each module is a Fibre Channel N_Port with exchangeable standard link cards (laser, LED or electrical). The modules are connected to a PC via a PCMCIA interface. They can be steered by dedicated programs that run in an MS-Windows environment.

The modules can be connected to N_Ports and F_Ports in different configurations, making it possible to use the tester for different purposes. It can work in six modes:

1. self tester
2. signal generator
3. N_Port tester
4. single or dual line monitor
5. fabric tester
6. fabric emulator

The first four working modes can be used with the present version of the tester, while the last two modes will be implemented later. The following sections present the working modes in more detail.

2.1 Self tester

With the self test program the functioning of the tester's hardware can be verified. Single and double module tests can be made that use an internal or external loopback to exclude or include the media drivers in the test. A set of predefined tests can be selected that can be run in any order.

2.2 Signal generator

The signal generator program (see figure 1) sends certain special character bytes continuously to the outgoing fibre. The user can choose from:

- FC 'comma' character used for testing byte synchronisation
- Minimum frequency (53.125 MHz) signal
- Two maximum frequency (132.8125 MHz) signals

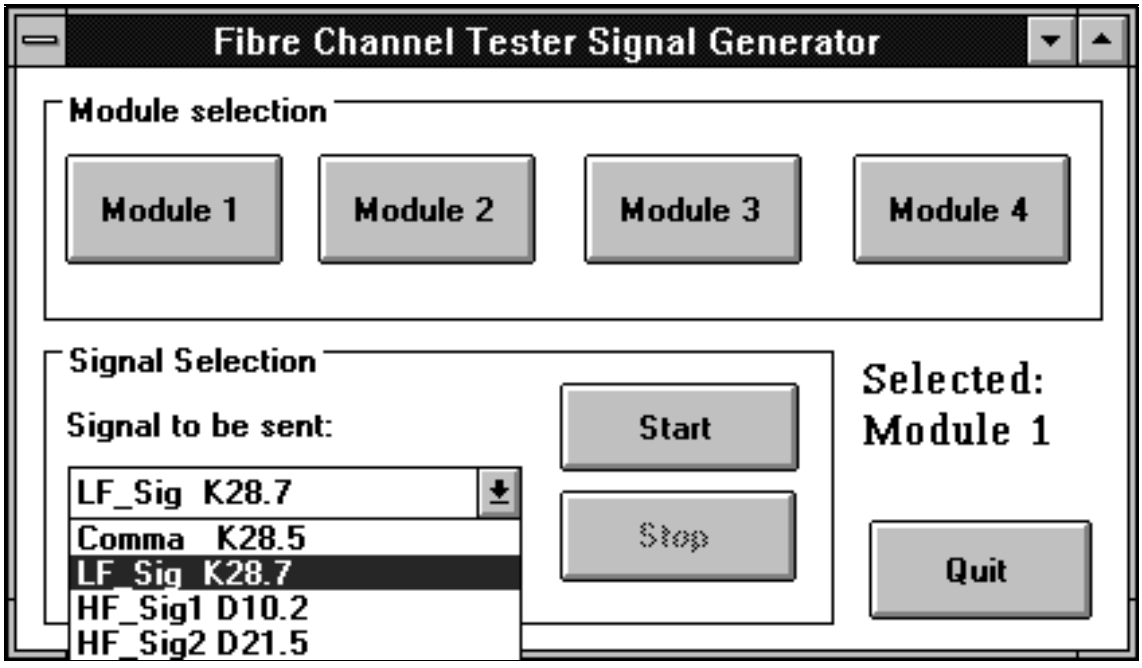

Figure 1: Signal generator user interface

2.3 N_Port tester

The N_Port tester program works with one module. It emulates an N_Port and can be used to test N_Ports such as computer interfaces or disk interfaces both at the link level and at the frame level. The tester can be an exchange originator or responder. The user can define correct and corrupted frames and sequences to send out. Also the user can define the correct or corrupted responses for frames arriving from the N_Port to be tested. A set of predefined frames and sequences can be used. All incoming and outgoing frames are displayed on the screen.

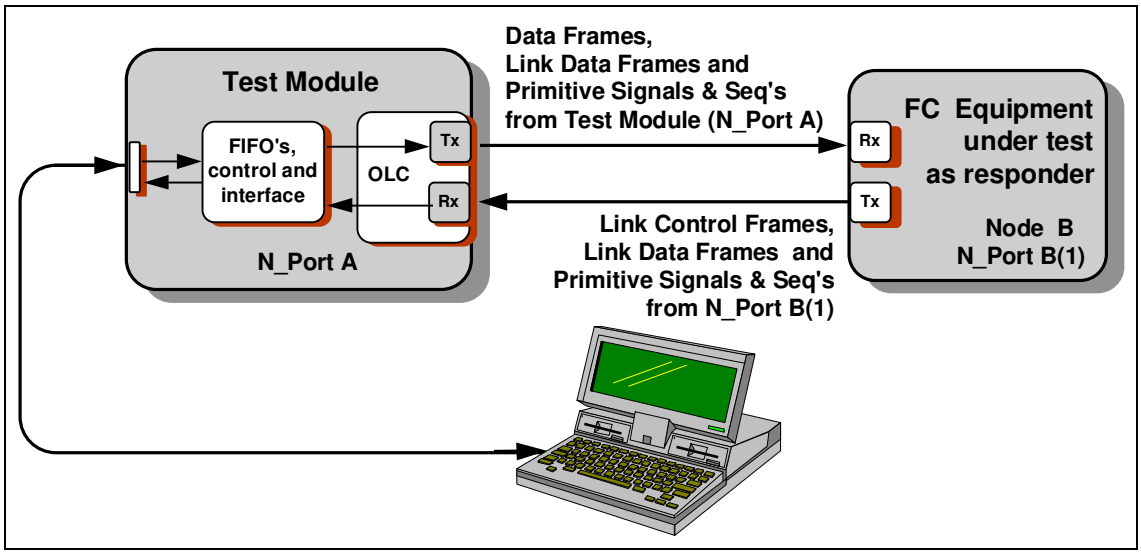

Figure 2: N_Port tester setup

To define the frames to send out, the user can call a frame editor. He can call up frames from a frame library as well. The frames can be chained to a sequence and the sequences to an exchange.

With the link level tests the correct functioning of the link initialisation handshake can be verified. A link level test consists of the definition of ordered sets to send out in response to a received ordered set or to the Start Test command. An ordered set is an FC term referring to four-character blocks that provide low-level link functions that are used for the signalling between two ends of a link.

A frame level test is defined by preparing the frames to send out in response to a given class of frames or to the Start Test command.

2.4 Line monitor

With the line monitor program the FC tester can be used as an FC analyser. It can monitor the data sent between two N_Ports. It can work with a single module or with two modules. In the latter case the data flowing over both fibres can be seen. Refer to figure 3 for an example of the setup. If the frame to be displayed contains information belonging to an upper level protocol mapped on Fibre Channel, then the program will recognise it and will display the upper level information accordingly. Figure 4 shows the user interface of the line monitor.

The line monitor program copies all information arriving at one receiver to the transmitter of the same or of the other module (according to the configuration).

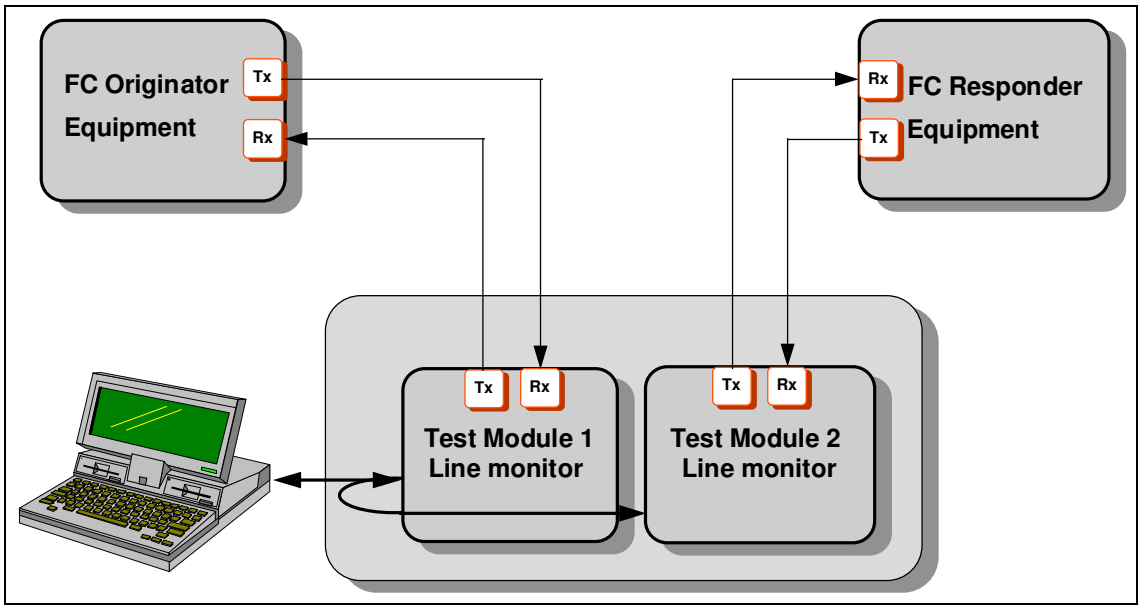

Figure 3: Dual line monitor setup

Frames arriving from one side are read into memory, stored in a buffer if necessary for the triggering, and sent out on the other side. The fact that the information passes through the computer slows down the exchange between the N_Ports. However, this does not decrease the suitability of the tester for finding bugs of protocol implementations or to do latency measurements.

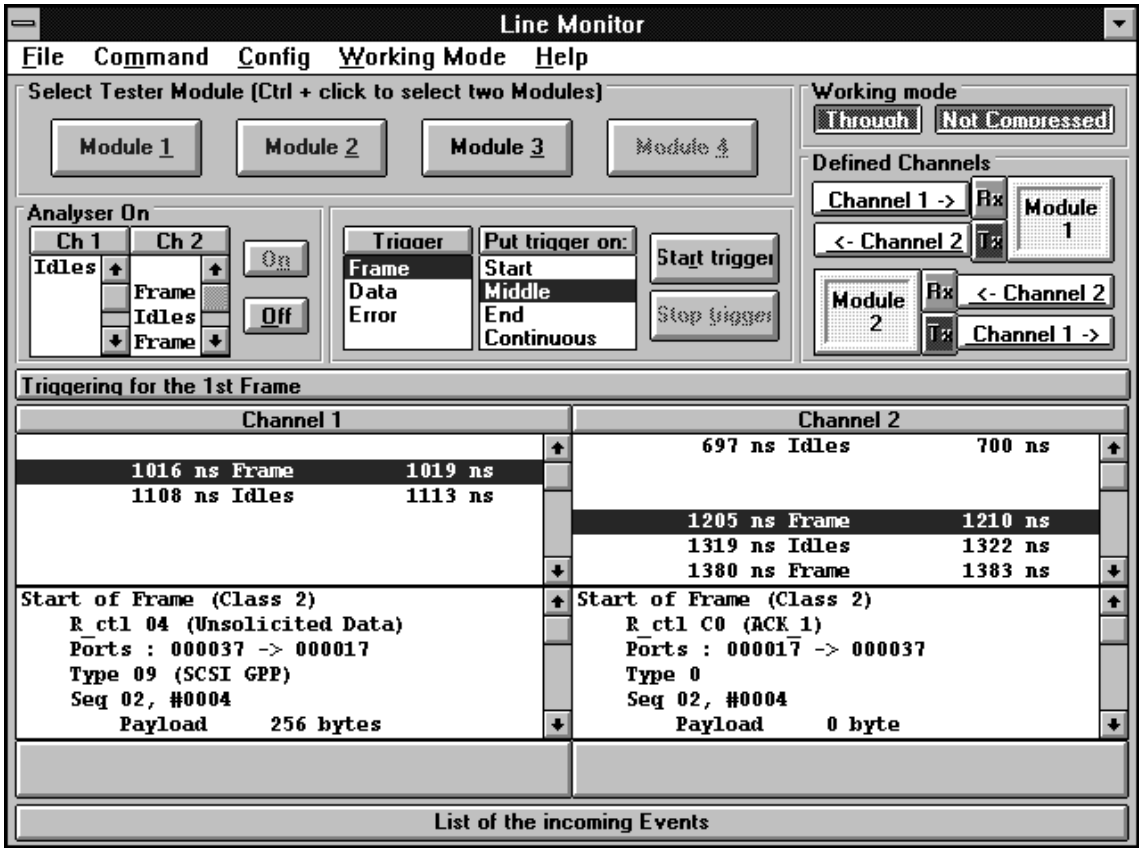

Figure 4: Line monitor user interface

2.5 Fabric tester

The fabric tester mode can be used to do simple performance measurements of fabrics. The tester can make accurate measurements of login latency and data transfer latency. As up to four test modules can be connected to one controlling PC, tests can measure the timing when several N_Ports are trying to send data to the same N_Port.

The same mode can be used to observe the behavior of the fabric in case it receives frames that are in error or that do not follow the Fibre Channel protocol.

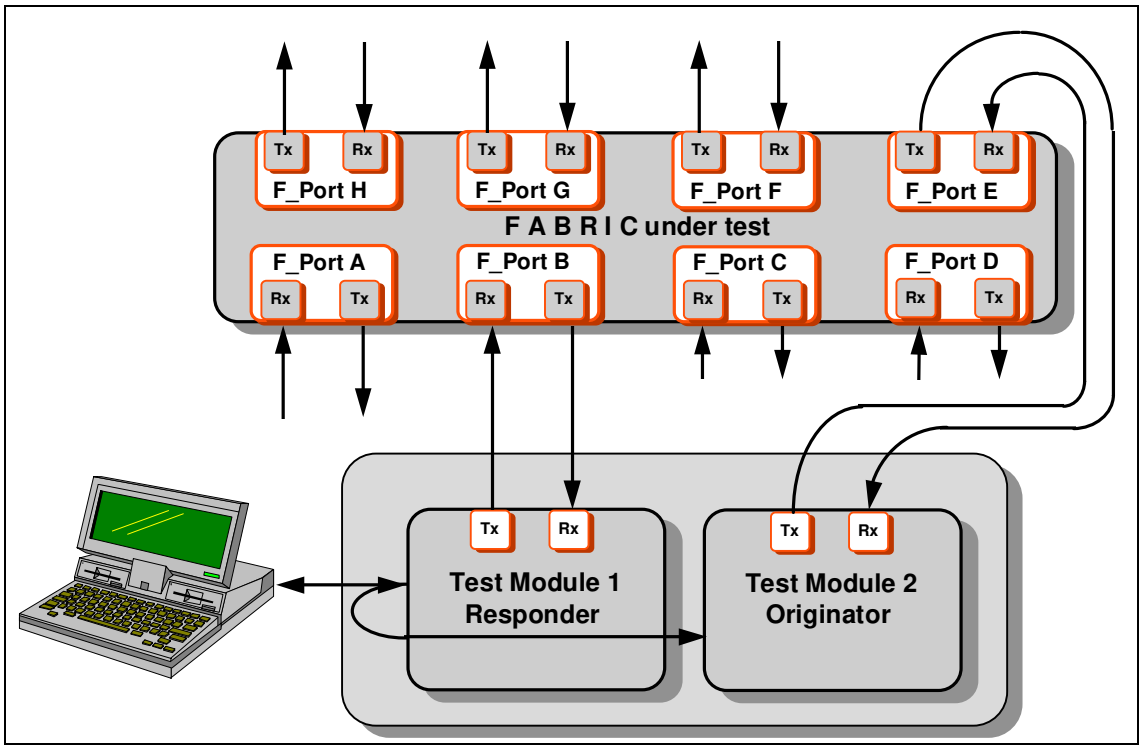

Figure 5: Fabric tester setup

2.6 Fabric emulator

In the fabric emulator mode the software on the tester will behave as a Fibre Channel fabric. The tester will be connected in a similar configuration as shown in figure 3. This fabric emulator mode can be used to test the behaviour of N_Ports when a fabric sends back frames that are in error or when it rejects frames. It can as well be used to measure latencies in an N_Port.

3. Tester hardware

The test module consists of five distinct parts: an interface to PCMCIA, an encoder/decoder (ENDEC), an exchangeable Optical/Electrical Link Card (OLC/ELC), transmitter logic and receiver logic. Figure 6 shows the simplified block diagram of the test module.

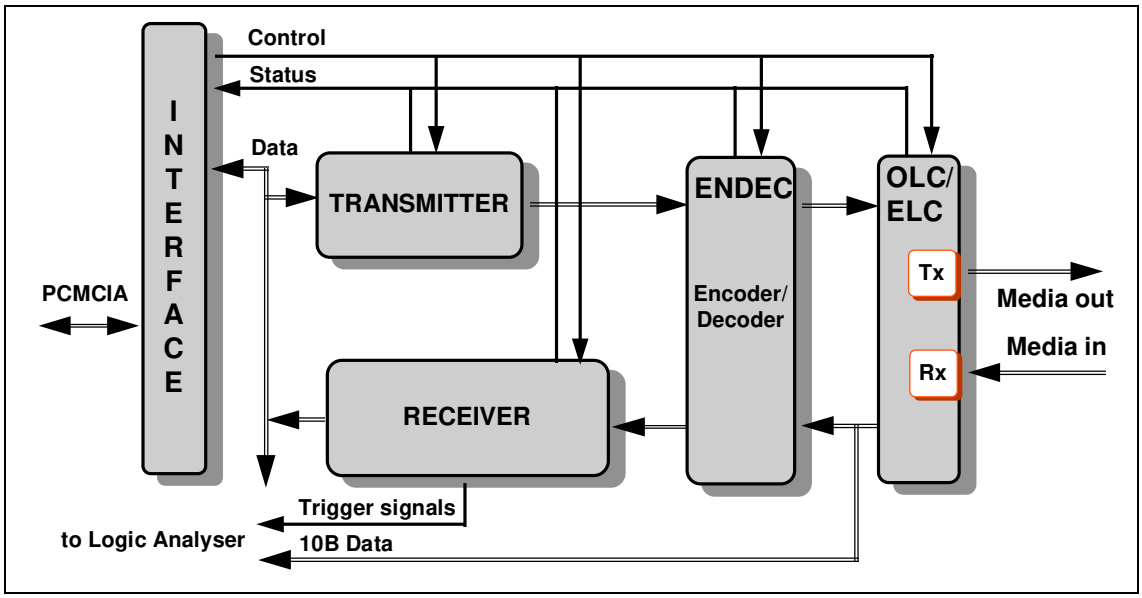

Figure 6: Simplified block diagram of the test module

3.1 PCMCIA bus interface

The PCMCIA bus interface can be split into two main parts:

- the PCMCIA interface that plugs into a PCMCIA slot of the controlling computer
- the command and register decoders with the control and status registers implemented in the test module board.

3.2 OLC/ELC

The OLC/ELC is a plug-in module that will serialise the 10-bit data and will transfer it onto the fibre. For the receive side, it will make 10-bit words from the serial data input stream. For this, it has a PLL which recovers the clock. It also detects the word boundary in the data stream. The OLC is the “Optical Link Card”, which can be bought from different manufacturers in both laser and LED versions. As part of this project we have developed an “Electrical Link Card”, so also the electrical variants of Fibre Channel can be tested.

3.3 ENDEC

The ENDEC, the encoder/decoder is a chip that will do low level Fibre Channel protocol processing. For the transmit side, it will take the 8-bit data from the transmitter and will encode it into 10-bit coded data. This so-called 8B/10B code ensures that the output data has a good dc-balance and a good transition density for easier clock recovery. For the receive side, it will do the decoding of the received 10-bit data into 8-bit data.

3.4 Transmitter logic

The transmitter logic (see figure 7) contains the following:

- 5k x 16 bits transmit FIFO:
  - sends single frames
  - sends multiple frames with idles between the frames
  - sends arbitrary data patterns
- 1k x 16 bits output status FIFO:
  - stores all events that have been sent on the outbound fibre with their time of occurrence
- link control logic:
  - sends single or multiple ordered primitive signals and sequences to the outgoing fibre
  - sends single or multiple undefined ordered sets to the outgoing fibre
- transmitter control logic:
  - controls the functioning of the transmitter
  - controls the data transmission from the transmit FIFO
- time stamp logic:
  - keeps track of the time of outgoing events

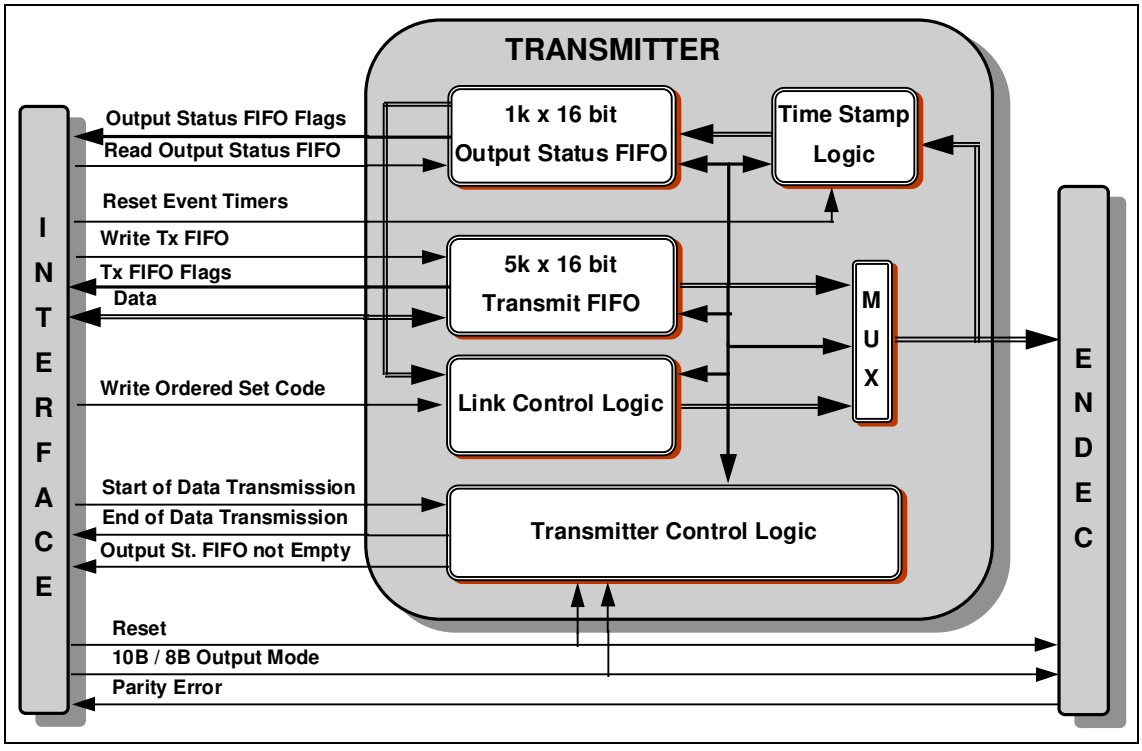

Figure 7: Simplified block diagram of the transmitter

3.5 Receiver logic

The receiver logic (see figure 8) contains the following:

- 5k x 16 bits receive FIFO:
  - stores complete frames

- stores only frame delimiters and frame headers in condensed receive mode
- stores status information for each received word

- 1k x 16 bits input status FIFO:
  - stores all events on the inbound fibre with their time of occurrence
- receiver control logic:
  - controls the functioning of the receiver
  - generates trigger signals for an HP logic state analyser
- time stamp logic:
  - keeps track of the time of incoming events

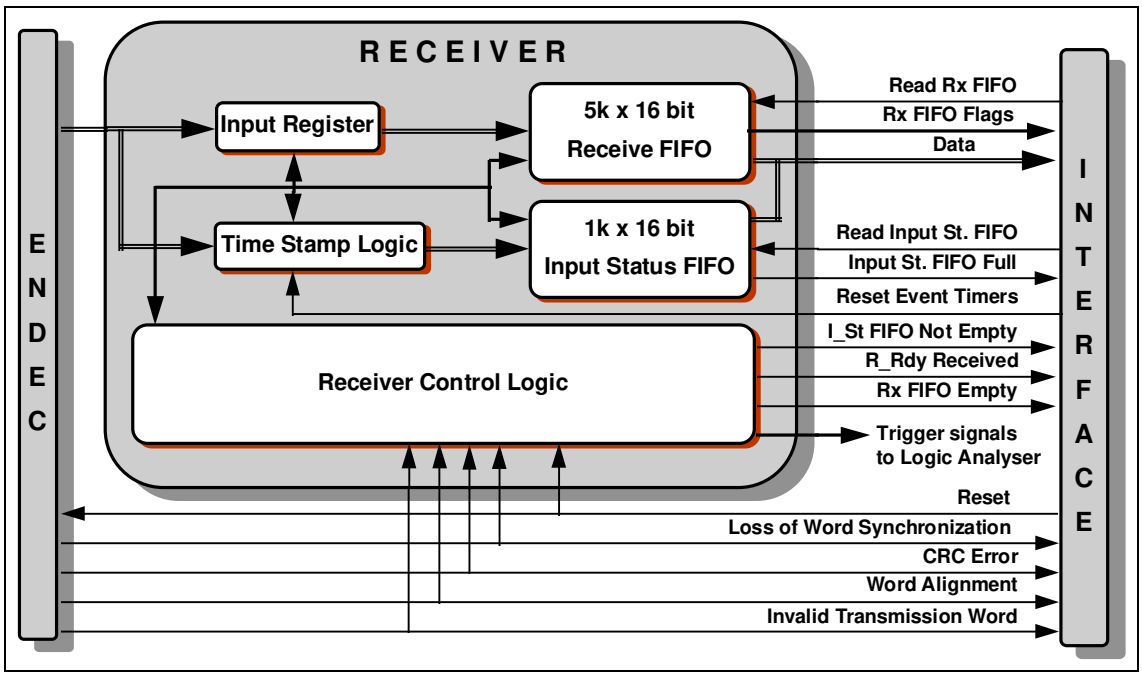

Figure 8: Simplified block diagram of the receiver

4. Tester software

The software of the Fibre Channel Test Box has been developed to run on a PC having a PCMCIA 2.1 interface. The software is written in Microsoft Visual Basic and Intel 80386 Assembly languages and runs under MS-Windows.

The program works in the following way: a 'supervisor' routine (main loop) permanently analyses a task list and decides which task to fulfil. Only if there is no urgent task, Visual Basic is allowed to react to user events. Selected events, such as the reception of a frame, arriving at the input fibre cause an interrupt. After returning from the interrupt routine the supervisor is called, i.e. the program investigates which task to complete before returning to the point where the interrupt arrived. The task list is made by the interrupt routines and by the main program. To realise the supervision of tasks we had to take over the interrupt service and stack manipulation from the Windows system. In this way we succeeded to utilise the advantages of MS-Windows and at the same time we could be sure that the urgent events are quickly serviced.

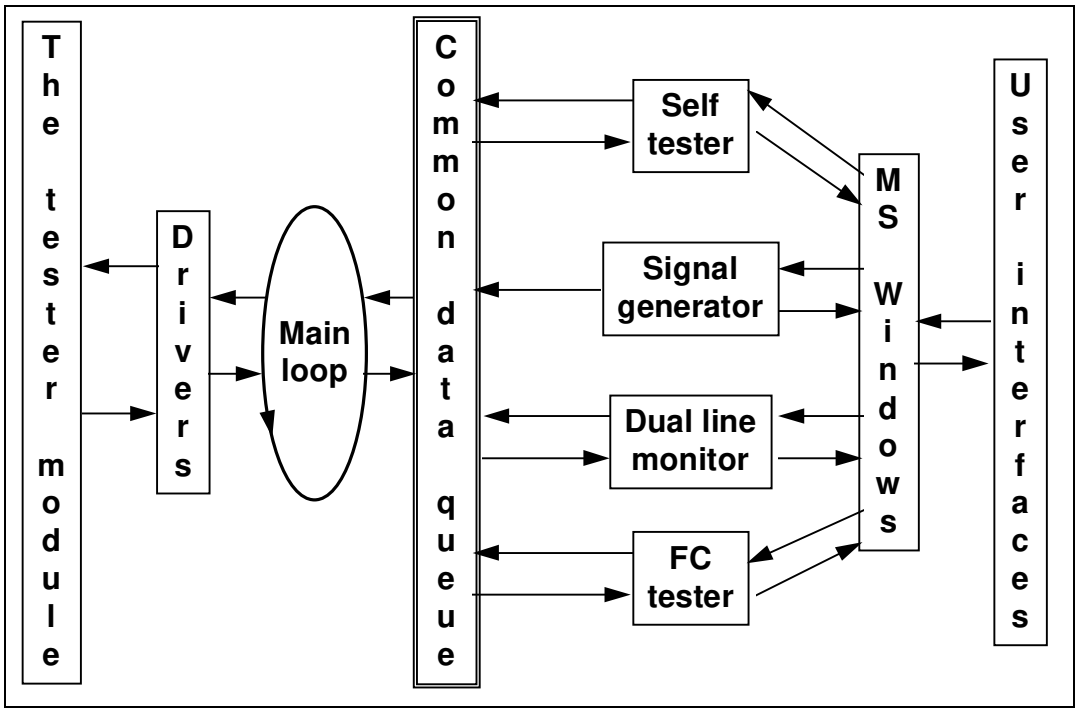

Figure 9: General organisation of the tester software

Figure 9 shows a diagram of the program organisation. The communication with the hardware module is done by drivers. They read the module's registers and FIFOs and copy the data to a common data queue or write the data from the queue to the module's registers and FIFOs. The drivers reading from the module are activated by interrupts from the module, the drivers writing to the module are activated by the user program.

5. Conclusions

The tester described has simple but flexible hardware and very powerful software. A wide range of testing procedures are supported, with the only limitation that the speed of the testing is low. The next version of the tester will reach the 1 GBaud speed group and by developing more complex hardware the speed of the tester will be increased significantly. At the same time the main directions of the software development will address the fabric emulation working mode and the support of testing of upper layer protocols, such as IP and SCSI.

References

[1] X3T9.3/Project 755D/Rev 4.2, "Fibre Channel Physical and Signalling Interface (FC-PH)", Working draft, ANSI, October 8, 1993.

[2] "Fibre Channel: Connection to the Future", The Fibre Channel Association, 12407 MoPAC Expressway North 100-357, P.O. Box 9700, Austin, TX 78758-9700, 1994.

[3] "The Fibre Channel Project Fibre Channel Test Box Software Specification", KFKI, Budapest, April 1994.

[4] "The Fibre Channel Project Fibre Channel Test Box Hardware Specification", KFKI, Budapest, April 1994.