A first-level calorimeter trigger for the ATLAS experiment

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Abstract

In the RD27 collaboration we have carried out system studies on the implementation of the first level calorimeter trigger processor system for the ATLAS experiment to be mounted at the Large Hadron Collider (LHC) at CERN. These studies suggest that the full system can be contained in six 18SU size crates which will process approximately 4000 electromagnetic and 4000 hadronic trigger cells and provide the central trigger processor (CTP) with signals from events with high-P_T electrons/photons, jets and missing-E_T.

A demonstrator trigger system operated successfully with the RD3 and RD33 calorimeters at the full 40 MHz LHC bunch crossing (BC) rate [1]. The prototype application-specific integrated circuits (ASICs) in this system each processed data from only a single trigger cell and its environment, which would lead to an extremely large system for ATLAS. Using eight-bit parallel data even the use of ASICs, processing multiple trigger cells would demand unacceptably large numbers of input pins and module connections.

Initial studies of this I/O problem produced a solution based on asynchronous transmission of zero-suppressed and BC-tagged data on 160 Mbit/s serial links [2]. This approach appeared to be feasible but would have introduced additional latency of about 20 BCs.

Further studies have led to the design of a fully-synchronous calorimeter trigger processor system using commercial high-speed optical links. The links will terminate in multi-chip modules (MCMs) incorporating custom-designed integrated optics, and the trigger algorithms will be implemented in ASICs.

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I. INTRODUCTION

The design luminosity of the LHC is 10^{34} cm^{-2}s^{-1}. At this luminosity the interaction rate is about 10^9 s^{-1} and with a bunch crossing every 25 ns there will be on average 18 interactions per crossing. The trigger system will have to analyse new data every 25 ns, and will have to achieve a rejection factor of about 10^4–10^5 without introducing any dead time. This requires a hard-wired processor operating in a pipeline mode.

The present plan for ATLAS is to have three levels of trigger (figure 1). Relatively crude decisions made quickly (less than 2 μs) at the first level can be refined at the second and third levels using more detailed information from the detectors.

Since the trigger decision takes longer than the interval between bunch crossings, the front end detector electronics has to incorporate pipeline memories to store the detector data until a level-1 trigger decision has been made.

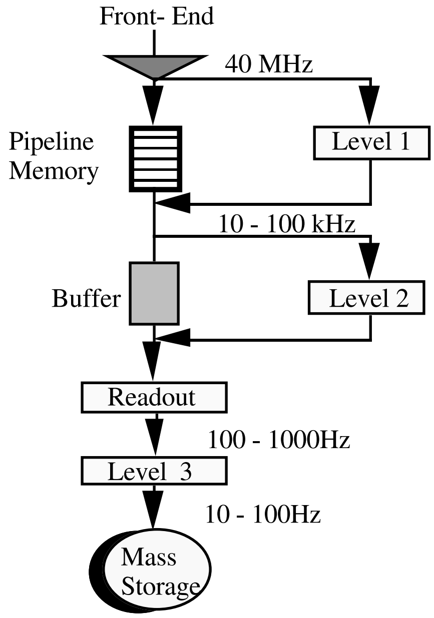

Figure 1: Multi Level Trigger Architecture

II. TRIGGER SYSTEM DESIGN

The first level calorimeter trigger processor system (figure 2) requires information from the calorimeter with a granularity of 0.1 × 0.1 in pseudo rapidity–azimuth (η- ϕ) space, giving approximately 4000 electromagnetic and 4000 hadronic trigger cells to process for $|\eta| < 3$.

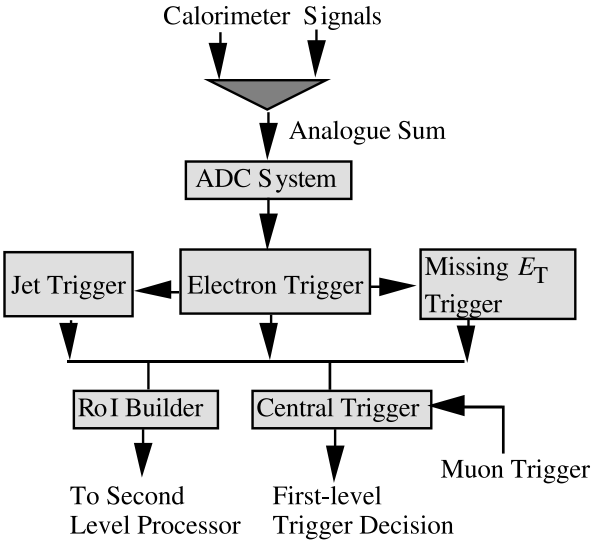

Figure 2: Trigger System Block diagram

III. ADC SYSTEM

The ADC system could be FERMI [3] or a custom built trigger ADC system independent of the calorimeter readout. If located on the detector it would transmit the digitised trigger information to the trigger processor system on fibre optic cables. The requirements of the trigger ADC system, as shown in figure 3, are as follows.

- Convert the analogue signal to eight bit digital signals at 40 MHz (corresponding to a 25 ns bunch crossing rate).
- Provide Look-Up Tables (LUT) for pedestal subtraction and calibration.
- Perform bunch crossing identification - see section IV.
- Combine pairs of eight bit trigger channels and convert to serial bit streams using 16 bit, 640 Mbit/s (data) parallel to serial converters (thus halving the number of optical links).
- Convert the electrical bit stream to optical signals.

IV. BUNCH CROSSING IDENTIFICATION

As the signals produced by the calorimeters are likely to span several bunch crossings, energy deposits originating in a single crossing would enter the trigger algorithms for several successive crossings. The role of the BCID logic would be to identify which data sample contains the peak of the calorimeter pulse, to pass on data for this sample only and suppress all other samples to zero.

BCID algorithms studied so far consist of a finite impulse response (FIR) filter followed by a peak-finding operation, as shown in figure 4.

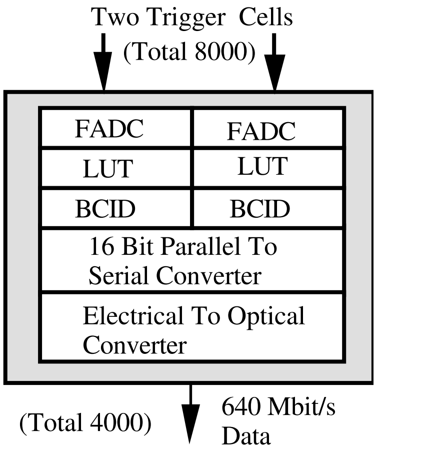

Figure 3: ADC System Block Diagram

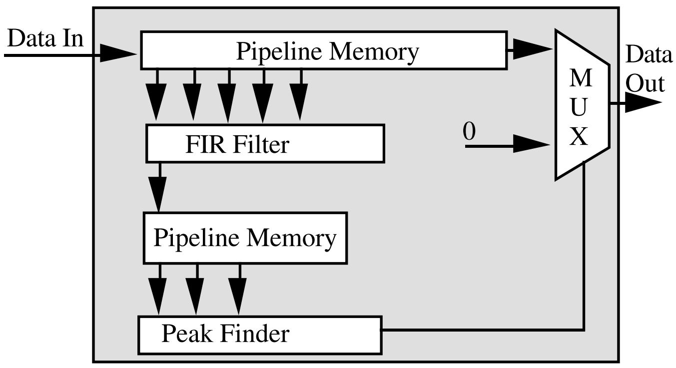

Figure 4: BCID Block diagram

V. ELECTRON PHOTON TRIGGER LOGIC

The most complex part of the trigger processor is the electron/photon trigger logic system (figure 5) which will receive 4000 optical signals from the ADC system.

In conjunction with industrial partners, a Multi Chip Module (MCM) containing integrated optical devices will be developed to receive the optical signals from the ADC system at an effective rate of 640 Mbit/s (800 Mbit/s including coding) from two trigger cells.

A single channel of the MCM (figure 6) will contain:

- An optical to electrical converter with a fibre pigtail (integrated optical device).
- A serial to parallel converter to translate the incoming serial bit-stream to a 16-bit word every 25 ns.
- A 4–bit × 4 serialiser, which will transmit the 16-bit word on four serial links operating at 160 Mbit/s, as required by the trigger algorithm ASICs.

- Readout memory to capture the input data.

The bare dies performing the above functions will be bonded and packaged as a single MCM, with the fibres passing through the side of a metal package. Each MCM will handle data from eight trigger channels.

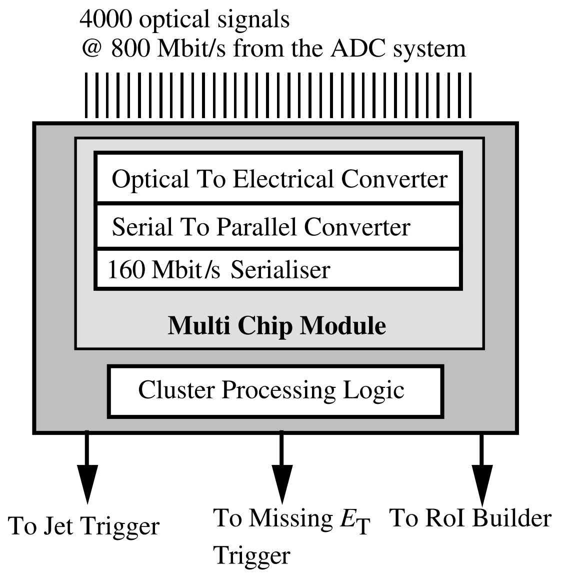

Figure 5: Electron/photon Trigger Block Diagram

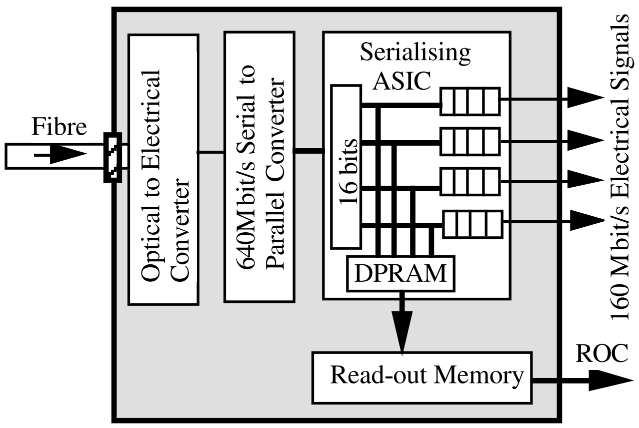

Figure 6: MCM Single Channel

The cluster-processing logic will form the heart of the calorimeter trigger. It will receive data from the above MCMs and compute the cluster hit pattern for de-clustering (section VIII), data for jet processing, data for missing-E_T calculations and Region of Interest information.

A. Electromagnetic Cluster Trigger Algorithm

Using 4×4 sliding windows within the calorimeter, the algorithm will search for isolated electromagnetic (em) energy clusters (figure 7).

The isolation requirement is based upon two E_T sums, one formed by the outer ring of 12 em cells and the other by all 16 hadronic cells.

The clusters are formed by considering a reference cell (2.2) within the 4×4 area and forming the four vertical and horizontal sums (2.2 + 3.2), (2.3 + 3.3), (2.2 + 2.3) and (3.2 + 3.3).

The trigger requirement is for at least one of these cluster sums to exceed a programmable cluster threshold and for both isolation sums to be below separate programmable isolation thresholds.

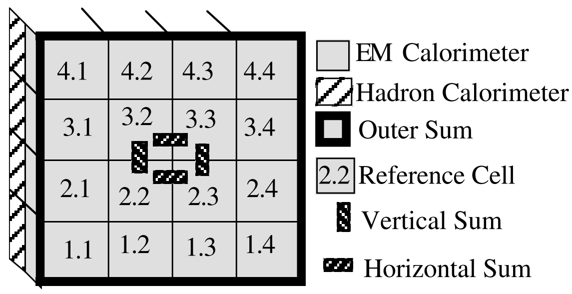

Figure 7: Area used for the algorithm

B. Cluster Finding ASIC

The most complex part of the logic required for the trigger processor will be implemented in the cluster finding ASIC, which will have the following features:

- Receive digitised information from the em and hadronic trigger cells using two serial links per trigger cell, each operating at 160 Mbit/s.
- Synchronise and perform serial/parallel conversion of the input data.
- Provide 16 processing elements per ASIC, which will require data from a 7×7 area of the calorimeters.
- Provide eight sets of threshold values (cluster and isolation thresholds) for the isolated em cluster trigger.
- Number of trigger cell input signals to the ASIC: $[(4+3) \times (4+3) \times 2]$ $\{\times 2$ links/cell$\}$ = 196 input signals @ 160 Mbit/s.
- Results:
  - Eight-bit region-of-interest (RoI), which is the 4×4 “RoI pixel array” for one threshold value locally de-clustered.
  - Eight-bit hit pattern, one bit per threshold, giving an OR over a 4×4 area for de-clustering (section VIII).
  - 13-bit transverse energy sum over a 4×4 area for missing-E_T calculations.
  - The 12 LSBs of the above sum serialised on to 3 links at 160 Mbit/s to be sent on to the jet trigger logic (section VII).
- Memory to capture the results (29 bits $\times$ 80 deep).
- Following a positive first-level trigger decision, the data corresponding to the appropriate bunch-crossing number should be transferred out from the dual port RAMs.

- The data I/O logic will use a 160 MHz clock and the core logic will run at 40 MHz.

The ASIC will be implemented in 0.5 micron CMOS technology. A total of 256 such ASICs will be required to process the entire em and hadronic calorimeters.

C. Cluster Processor Board

The Cluster Processor board will fully process an 8 × 8 area of the em and hadronic calorimeters. Each board will contain 16 MCMs receiving optical data at 640 Mbit/s on 64 optical fibres, four Cluster ASICs, LUTs to convert the energy to its E_X and E_y components, two Adder ASICs for forming the energy sums, and other control and interface functions to communicate with the read out controller.

Fan-in and fan-out of data between neighbouring boards will be carried out using a high speed transmission line backplane at 160 Mbit/s.

A total of 64 Cluster Processor boards will be required for the complete trigger system (16 boards/crate × 4 crates).

VI. MISSING E_T LOGIC

The missing-E_T calculation will start on the Cluster Processor boards, where E_X and E_y components of the total energy in the fully processed 8 × 8 area of the calorimeter will be calculated. Further calculations will be carried out on two other boards, namely the Results board and the Missing-E_T board.

There will be 16 Cluster Processor boards in a crate, each calculating E_X and E_y components. A Results board in each crate will carry out further summing using an Adder ASIC. Each Cluster Processing crate will require two Results boards to sum the E_X and E_y values respectively. These sums will be transmitted to the Missing-E_T board.

The function of the Missing-E_T board will be to receive the partial E_X and E_y sums from the eight Results boards (2 Results boards/crate × 4 crates), carry out further additions using the Adder ASICs and then test $E_T = \sqrt{(E_X{}^2 + E_y{}^2)}$ against four thresholds to provide a 4-bit E_T hit flag to the central trigger logic. A single Missing-E_T board will be required in the system to carry out the above functions.

VII. JET TRIGGER LOGIC

The jet algorithm will be performed using the energy sums over the 4 × 4 areas of the calorimeters calculated in the Cluster Processing boards. These sums will define jet trigger cells of granularity $\Delta\eta \times \Delta\phi = 0.4 \times 0.4$. The algorithm will then calculate the total energy in a 2 × 2 sliding window of such jet trigger cells and compare the sum with eight threshold values.

To implement the algorithm a Jet ASIC will be designed in 0.7 or 0.5 micron CMOS technology to fully process eight such sliding windows. With four Jet ASICs per Jet Processing board, each board will then process 32 jet windows, receiving the necessary information from the Cluster Processing boards on balanced ECL serial links operating at 160 Mbit/s. The full system will require a total of 32 Jet ASICs and eight Jet Processing boards.

As in the case of the em cluster processing, the effect of overlapping sliding windows implies that some information must be shared over the crate backplane between Jet Processing boards.

VIII. DE-CLUSTERING LOGIC

The electromagnetic cluster finding algorithm and the jet algorithm described above are based upon a sliding trigger cell window. Since the windows overlap, double counting could occur when counting the hits.

The function of the de-clustering electronics is to count the hits once by applying a 'veto pattern' to the hit patterns and to count only the non-vetoed hits.

The de-clustering electronics for jets and em clusters will be identical, and will provide the following functions:

- Receive the 256 pixel array (hits) from either the Cluster Processor boards or the Jet Processor boards.
- Apply vetoing and count non-vetoed pixels.
- Compare multiplicity with eight threshold values.

Part of the vetoing and counting logic will be implemented on a Veto ASIC which will veto and count the em clusters/jets from a 4 × 4 pixel array. The vetoed pattern will be saved in a dual port memory to be used for jet RoIs.

Using 16 Veto ASICs and five Adder ASICs per board to complete the adder tree, the system will require a total of sixteen De-clustering boards to process the em clusters and jets.

IX. READOUT CONTROLLER

Each crate will require a Readout Controller (ROC) to enable the host computer to communicate with the boards and also to provide an interface to the second-level trigger for transferring the RoI information.

The ROC will have a processor to control and format the data which may also provide test facilities. For example, when idle it may perform a software cluster algorithm on the data received from the boards. The test results could be recorded in a status register to be read out by the host computer.

X. TESTING AND MONITORING

The system will provide test and monitoring facilities by incorporating FIFO “spy” buffers at the input and output of a board, allowing the data to be read out for analysis. The processor in each ROC may also perform data analysis on all the boards in the crate and set a flag to enable the host computer to identify faulty boards. Since all the crates will have a ROC, the complete system can be monitored in this manner.

XI. SYSTEM CRATES

Each Cluster Processor crate will process 1000 em and 1000 hadronic trigger cells and will include: 16 Cluster Processor boards, two Results boards and a Readout Controller. Four crates will be required for the cluster processor logic.

The Jet Processor crate will include eight Jet Processor boards, eight De-clustering boards and one Readout Controller board.

The em De-clustering crate will include eight De-clustering boards and one Readout Controller board. The Missing-E_T board will be housed in one of the spare slots in this crate.

The system will make use of 18 SU size crates (1 SU = 25 mm) with 21 slots per crate.

XII. DEMONSTRATOR PROGRAMME

An intensive R&D programme has been pursued over the last three years with the general aim of exploring the problems of a digital implementation of a calorimeter trigger at level-1.

A. Cluster Finding Logic

In phase one of this programme we designed an ASIC using 0.8 micron CMOS gate array technology [4] to implement a cluster finding algorithm. A demonstrator system incorporating this ASIC was successfully tested in CERN test beams with the RD3 and RD33 calorimeters [1].

B. BCID Logic

To implement all the BCID algorithms previously studied in simulation a single-channel BCID demonstrator module was constructed and successfully tested with the RD3 liquid argon calorimeter in a test beam at CERN [5].

Building on this work, a second demonstrator system is now being designed with the BCID algorithms implemented in Xilinx field-programmable gate arrays (FPGAs). With four channels per FPGA, BCID will be performed on 36 calorimeter channels in a CERN test beam in 1995.

C. Integrated Optics, MCM and Backplane

A fully synchronous level-1 calorimeter trigger system as described above can be realised using only six crates of electronics. The viability of a such a system depends crucially on three areas: the MCM, the integrated optical device and the high density high speed backplane providing data fan-out at 160 Mbit/s.

All these areas will be studied in phase two of the demonstrator programme, with beam tests at CERN in 1996.

XIII. SUMMARY AND CONCLUSIONS

The first-level calorimeter trigger system will process 4000 electromagnetic and 4000 hadronic trigger cells, and will provide the following sub-triggers to the central trigger logic:

- EM cluster (electron/photon) trigger with eight sets of programmable cluster and isolation threshold values, each with several programmable multiplicity thresholds.
- Jet trigger with eight programmable threshold values, each with several programmable multiplicity thresholds.
- Missing transverse energy trigger with four threshold values.
- Apart from providing the above sub-triggers to the central trigger logic, the system will provide Region-of-Interest information to the second-level trigger, and allow intermediate results to be read out for off-line evaluation and monitoring.

With a total of 103 modules, the system will require six 18 SU crates, and involve six circuit board designs and five ASIC designs. The system can be implemented using technology which is either already available or which will be available in the very near future.

A demonstrator programme is planned to prove the crucial elements in the design, at the conclusion of which a full system design will be undertaken, followed by a prototyping phase and the production of the final system modules.

XIV. REFERENCES

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[5] I. P Brawn et al., Beam Test of a Single Channel Bunch Crossing Identification Module for the Level-1 Trigger, RD27 note 31, October 1994.