the 4 x 8 region. Section 4.7 itemizes the 304 lines required by the Electron Isolation card. A 340 pin AMP stripline connector will be used as the main data connector. The additional pins beyond 304 will be used to forward the results to the Jet Summary card and to input clock and control information. As in the case of the Receiver card, the top part of Electron Isolation card will use a 128 pin DIN connector to interface to a 32 bit VME bus.

5.2 Isolation

The algorithm used to determine isolation examines the individual sums of a reference tower with its four nearest neighbors. The maximum sum is chosen and two cuts are applied on the longitudinal and transverse isolation of the ECAL energy deposit. The first cut requires the central tower HCAL to ECAL energy ratio to be < 0.05. The cut on transverse isolation requires the sum of HCAL transverse energy in the eight nearest neighbors to be ≤ 2.0 GeV. In order to reduce the number of bits exchanged between cards, we limit the dynamic range of neighboring HCAL information to 2 bits. Overflows of any of the energy ranges are treated as maximum values. An option is being considered to include electromagnetic isolation by requiring the energy in one of 4 corner-centered combinations of 5 ECAL towers to be less than 2.0 GeV.

The input data is staged on the Receiver card to arrive in a particular order in time at the Electron Isolation card. Careful data organization makes it possible to process the data as it is being received, rather than storing it for a full crossing to use in parallel on the card. The Isolation ASIC is designed to shift in the data for 16 towers, 4 towers at a time, over a single bunch crossing time. The data for the 20 neighboring towers is also be loaded in the same time period. The entire 4 x 8 region is processed by two ASICs in four 160 MHz cycles. A detailed description of the order of the data is given in section 5.2.1.

The output of the ASIC is four 2-tower sums, with eight bits of dynamic range, and four 1-bit results indicating whether the eight nearest neighbor hadronic sums are ≤ 2.0 GeV. These results are produced every 6.25 nsec. In parallel with the Isolation ASIC are a set of lookup tables which use the same input information to determine H/E for each of the reference towers. The four 2-tower sums from the Isolation ASIC are combined with the two single bit results from the hadronic sum and H/E cuts and presented to a programmable look-up table which ranks the electron trigger results.

These ranks, one per reference tower, are presented in parallel to a single Sort ASIC. The Sort ASIC receives all 32 ranks from the two Isolation ASICs in one crossing and appends 5 bits of location information to each input. The 5-bit location follows each datum through the Sort ASIC and uniquely identifies the four largest. The resultant from the ASIC is the four highest ranks from the 4 x 8 trigger tower region. There is a four crossing latency for the result, but the pipeline architecture ensures that, once filled with data, a new result will appear every crossing.

5.2.1 Isolation ASIC

The Isolation ASIC, shown in Figure 13, handles four electromagnetic energies (A_{in}, B_{in}, C_{in}, D_{in}) on an 8 bit scale, every 6.25 nsec. Nearest neighbors are also included in the data flow. During the first cycle of every crossing the four neighboring energies (TE_A, TE_B, TE_C, TE_D) from the adjacent 4 x 4 region (top) are also be strobed into the ASIC. The neighbors along either edge of the 4 x 4 region (LE_{in}, RE_{in}) are also included, two at a time (left and right edges), during each 6.25 nsec period. Finally, the last cycle strobes in the four neighboring towers of the bottom edge (BE_A, BE_B, BE_C, BE_D). The nearest neighbor corners are not required by the algorithm. Thus, in one bunch crossing time, a total of 36 towers are clocked into the Isolation ASIC. All the neighboring electromagnetic energies are provided as the top 6 bits of the 8 bit range used for the reference towers.

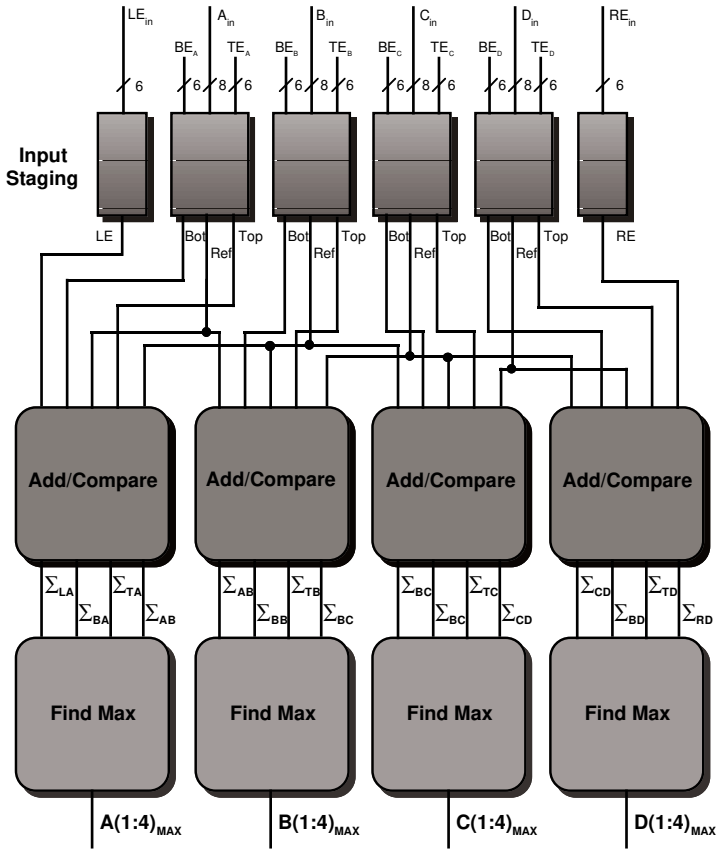

Figure 13. Block diagram of the Electron Isolation ASIC.

Separate inputs are used to clock in the top and bottom neighboring towers in order to avoid unfavorable routing or extra components on the board due to board level multiplexing. The top and bottom neighboring edges require a total of 2 x 4 x 6 = 48 input pins. The central region needs 4 x 8 = 32 input pins, and the left and right edges need 2 x 6 = 12 pins. The total number of data inputs is 92 pins, for a total of 36 towers of information. In addition pins

are allocated for reset and clock inputs. All signal I/O, with the exception of the clock, is single-ended.

The Isolation ASIC also handles the hadronic tower data, as discussed in section 5.2.1.4, necessary to check for hadronic isolation around individual towers. All neighboring hadronic information is on a 2 bit scale. Again, the data is shifted into the ASIC on 6.25 nsec cycles. The central 4 x 4 region requires 4 x 2 bits, or 8 pins, for each cycle. The top and bottom edges are entered on separate inputs, requiring a total of 2 x 6 x 2 bits, or 24 pins. The factor of six is necessary because the nearest neighbor corners are included in the determination of hadronic isolation. The left and right edges need an additional 2 x 2 bits, or 4 pins, to complete the count. The total number of pins required for the hadronic data is 36.

The only outputs are the four electromagnetic and four hadronic results. Four two tower sums, on an 8 bit scale, and four corresponding 1 bit hadronic isolation flags are produced each 6.25 nsec. One crossing is required to output the results for the entire 4 x 4 array. The total number of output pins is 36. The combined total of inputs and outputs, including control signals, is 170 pins. Since the ASIC is essentially a dataflow device, there is very little in the way of control logic or control lines needed for the operation of the chip.

5.2.1.1 Input Staging

The Isolation ASIC processes the data through three separate blocks. The first of these, the Input Staging, is illustrated in Figure 14. The purpose of this block is to receive the data at the time when it is available and change the time relationship to be suitable for the processing that follows. Only one column of input data is represented in the figure.

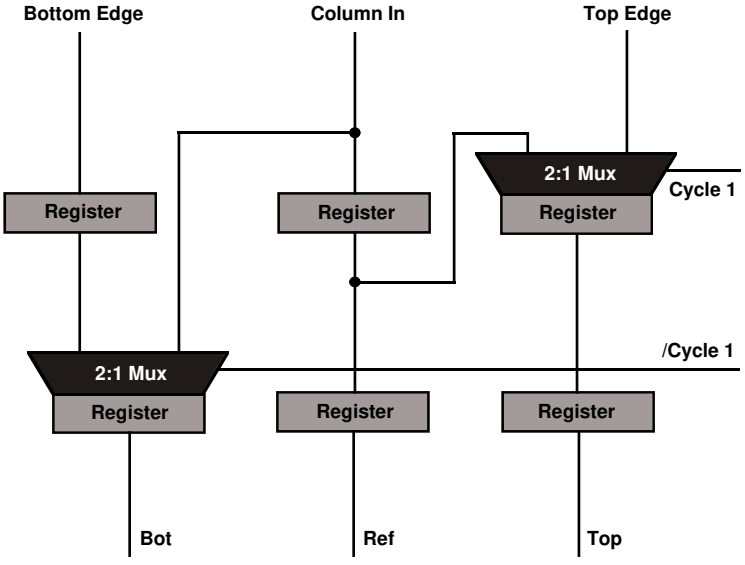

Figure 14. Isolation ASIC input staging.

At the beginning of a crossing, the first row of the 4 x 4 array is available, along with the top edge. The signal **Cycle 1** selects the **Top Edge** input on the right hand multiplexer. After the first 6.25 nsec clock, the first rank of registers contain one of the towers in the 4 x 4 array (a reference tower) along with its top neighbor. The left-most register in the top rank is undefined at the beginning of the sequence. After a second clock cycle, the reference tower is in the middle register of the bottom rank of registers and its top neighbor is in the right hand register. The left-most register in the bottom rank contains the next successive reference tower, as does the middle register in the top rank. This value in these registers is the bottom nearest neighbor for the first reference tower. The sequence continues to the cycle where the last reference tower in a column of 4 towers is clocked into the middle register in the bottom rank. During the same cycle the **Bottom Edge** data is available from the neighboring card. It is clocked into the bottom left register during **Cycle 1** at the beginning of the next sequence.

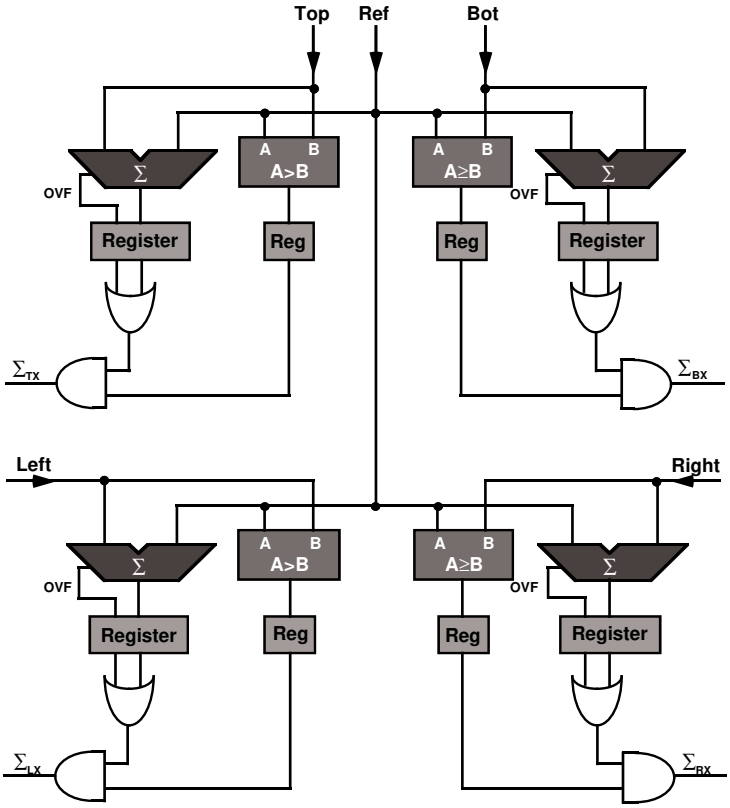

Figure 15. Electron Isolation ASIC Add/Compare block.

Once the pipeline has been filled, data will continue to be output from the Input Staging block four towers at a time each with their corresponding top and bottom neighbor. The left and right neighbors are either the adjacent reference towers in the 4 x 4 array or the left and right columns of data from neighboring boards.

5.2.1.2 Add/Compare

The Input Staging block places each tower and its neighbors in the same time frame. The remaining blocks in the chip can now handle the processing in parallel. The function of the Add/Compare block, shown in Figure 15, is to form four sums between a reference tower and its top, bottom, left and right neighbors. At the same time the sums are being formed, four compares are made to determine for each pair of towers whether the reference tower is larger than or equal to its neighbor. In the case of comparison with the top tower, the reference tower must be greater than the top. When compared with the bottom tower the reference tower must be greater than **or** equal to the bottom. The different conditions used to check for inequality with respect to the top and bottom towers is imposed to remove the possibility of double counting when two towers, one above the other, are equal. This does build a bias into the circuit in that the bottom tower, of an identical pair, is always taken as the reference tower. The same process is used to guard against double counting in the left to right direction.

When a tower pair satisfies the equality check the sum from the adder is enabled to the Find Max block. When the sum is disabled, a value of zero is passed on to the next block. If the adder has overflowed (carry out equals one) the results of the addition are set to FF_H.

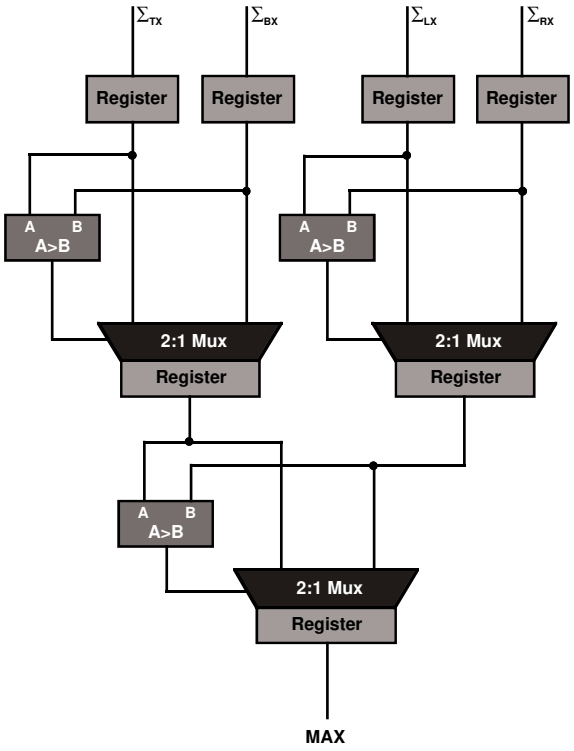

Figure 16. Electron Isolation ASIC block which determines the maximum pair.

5.2.1.3 Find Max

The last stage in processing the electromagnetic information, the Find Max block, is shown in Figure 16. The four sums (Σ_{TX}, Σ_{BX}, Σ_{LX}, and Σ_{RX}) are presented, in parallel, to two comparators. The outputs of these comparators are used to select the maximum of each pair which are placed in intermediate storage. These two maxima are presented to a single comparator during the next clock cycle. The output of the comparator is used to select the maximum. The single maximum from the original four values is stored in the bottom register shown in Figure 16.
The total latency for the electromagnetic data path is 7 x 6.25 nsec or 1.75 bunch crossing times. It is likely that detailed simulation will show the register at the input of the Find Max block can be removed. This would reduce the latency to 1.5 bunch crossings.

5.2.1.4 Nearest Neighbor Hadronic Sums

The hadronic information enters the ASIC in the same time frame as the electromagnetic information. Some staging is necessary on the board to put the four corner towers from neighboring boards into the proper time sequence. Figure 17 illustrates the section of the chip that checks the hadronic isolation.

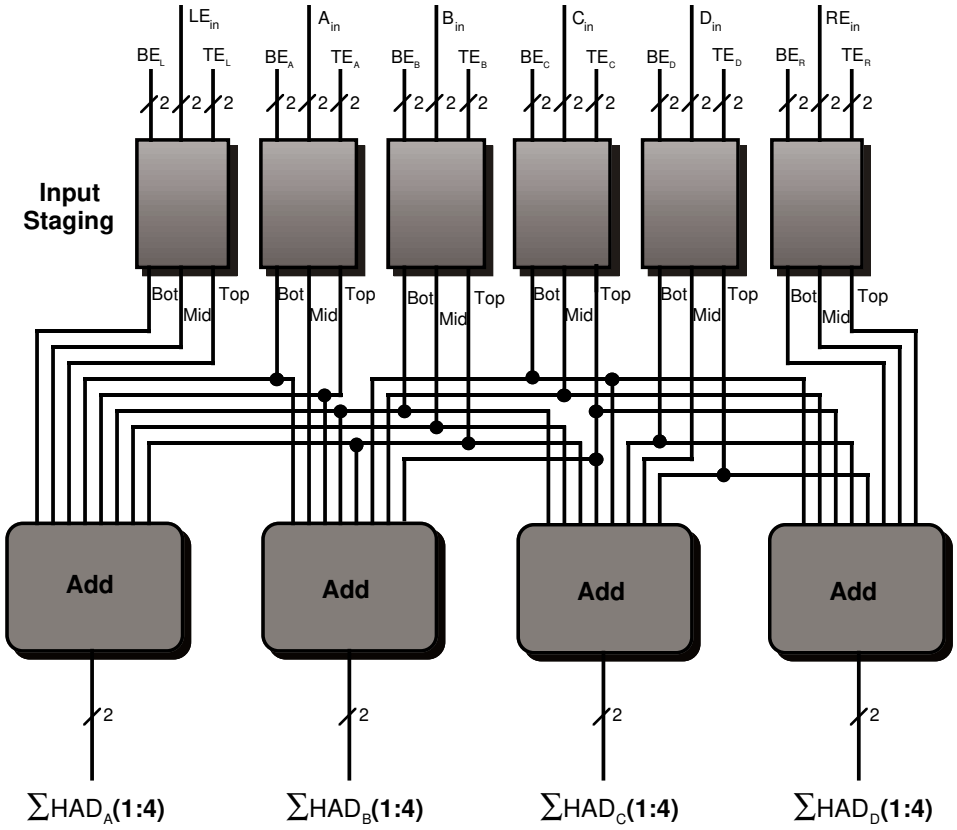

Figure 17. Electron Isolation ASIC Hadronic isolation block.

The same Input Staging design as that used in the electromagnetic processing section is used to put reference towers and nearest neighbors into the same clock cycle. Two cycles (12.5 nsec) after entering the ASIC, the data is presented in parallel to four 8-operand adders. Each operand has a resolution of 2 bits. Details of the adder block are not shown. The adder blocks are implemented as binary trees, each reducing the original 8 operands to one in three 6.25 nsec cycles. The result from each adder block will be checked for ≤ 2.0 GeV and a single bit set to indicate the sum has passed the cut. The output of this bit will be timed in to coincide with the output from the electromagnetic processing section of the ASIC.

5.2.1.5 Boundary Scan

It is our intention to implement the same controller and instruction decoder for boundary scan as used in the Adder ASIC. All ASICs in the Level 1 trigger processor will have compatible boundary scan circuits.

5.3 Lookup Tables

Lookup tables are used for two separate functions. The first is to calculate the H/E cut. This operation is performed in parallel with the processing in the Isolation ASIC. Eight memories, cycling at 160 MHz, receive the same data as that shifted in to the reference tower locations in the Isolation ASIC. Only the top 4 bits of the 8-bit electromagnetic data are used. Simulation studies indicate that full resolution on E_T is not required [5]. The four bits of the hadronic information is combined with the four bits of electromagnetic information, producing an 8-bit address into the H/E lookup table. A single output bit is used to indicate, when true, that H/E < 0.05. The full 4 x 8 trigger tower region is processed in one crossing, which is slightly less than the time required by the Isolation ASIC. The H/E bits will be delayed a sufficient number of cycles to ensure they are available at the same time as the corresponding sums and hadronic isolation bits are available from the Isolation ASIC.

A second set of lookup tables are used to produce a ranking of the electron trigger information based on the 8-bit sums, hadronic isolation from the Isolation ASIC, and the single bit result from the H/E cut. These 10 bits are used as an address into the lookup tables and will produce a value of 6 bits in length which represents a ranking of the different trigger categories resulting from the data. The memories will be cycled at 160 MHz. Therefore, one bunch crossing is required to produce the ranking information for the 4 x 8 region.

5.4 Sort

In order to limit the amount of information transmitted from each Electron Isolation card and each regional trigger crate, we have chosen to send only the four highest ranked trigger categories from each Electron Isolation card to the

Jet Summary card. These four values have not been put in any particular order. Jet Summary card receives a total of 32 values from 8 Electron Isolation cards and sorts these again to determine the four largest values. The E_T information sent to the Jet Summary card from the Receiver card is also sorted to determine the four 4 x 4 subregions with the largest energy deposition.

5.4.1 Sort ASIC

The Sort ASIC is designed to find the four largest of thirty-two 10-bit values. Ten bits is sufficient to handle both the E_T sums and the trigger category information. Figure 18 is an illustration of the major functional blocks that make up the ASIC. Rather than try to design an ASIC that will handle thirty-two 10-bit operands in parallel, it was decided to shift the data in, eight operands at a time, over four 6.25 nsec cycles. This matches the rate at which data is coming from the lookup tables and reduces the number of input pins from 320 to 80.

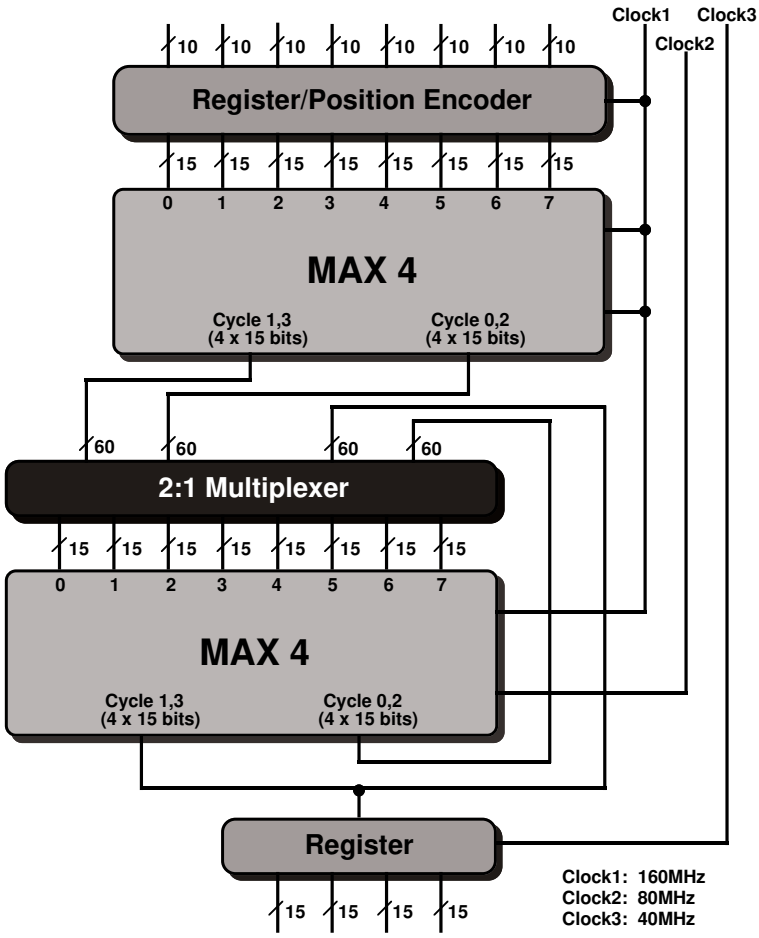

Figure 18. Sort ASIC block diagram.

The algorithm implemented within the Sort ASIC is based on a simple rotation of operands and is shown schematically in figure 19. The eight

operands are divided into two groups of four. The operands are compared in pairs between the two groups, with the larger of the two taking over the position of the left hand member of the pair. This comparison is performed in four stages with a rotation of compared pairs occurring between each stage. By the end of the fourth stage a sufficient number of comparisons have been made to ensure the four largest values are in the left-hand group. In order to save steps, and thus minimize the total latency, these four values are not placed in any rank order. The final four values, produced by the global trigger processor, are ordered during the final sort.

5.4.1.1 Register/Position Encoder

The first functional block of the Sort ASIC is the Register/Position Encoder. The main purpose of this block is to provide storage for the incoming data to isolate it from board propagation delays. It is also used to append 5 bits of positional information to each of the operands as they arrive at the chip. The position is based on the which input (1 of 8) and which cycle (1 of 4) the data coincides with. The cycle number is derived from a 2 bit counter which is initialized via a reset at startup time. The two values, position and time, are concatenated to produce the 5 bit value.

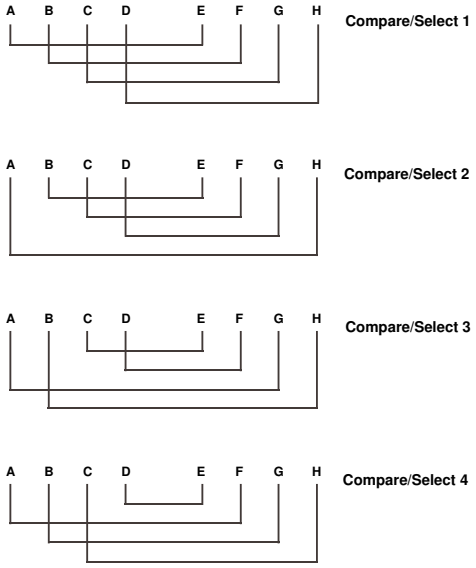

Figure 19. Sort ASIC compare pattern.

5.4.1.2 MAX4

The next block in the sequence is the MAX4 block. A more detailed picture is given in figure 20, which shows that the block is isolated from the previous block with a register. This level of register may not be required; it is included pending simulation results on its necessity. The rest of the MAX4 block is made up of four Compare/Select blocks. One of these blocks is illustrated in greater detail in Figure 21. Each of the four blocks is different from its neighbor in that each has one of the four stages of pairing, shown in Figure 19, for the compare hardwired in the circuit.

The Compare/Select block performs all four compares in parallel. Fifteen bits arrive and leave at the inputs and outputs. The top five bits are the positional information mentioned above. They are carried along with the data through the 2:1 multiplexers. The bottom 10 bits (raw data) are used by the compare to drive the select lines of the multiplexers. Each pair of multiplexers has the same operand wired to opposite inputs. The results from the compare force the left hand multiplexer to store the larger of the two values and the right hand multiplexer to store the smaller of the two. After one 6.25 nsec clock cycle the eight operands have been reorganized with the larger of each pair of values stored in the registers in the left hand column.

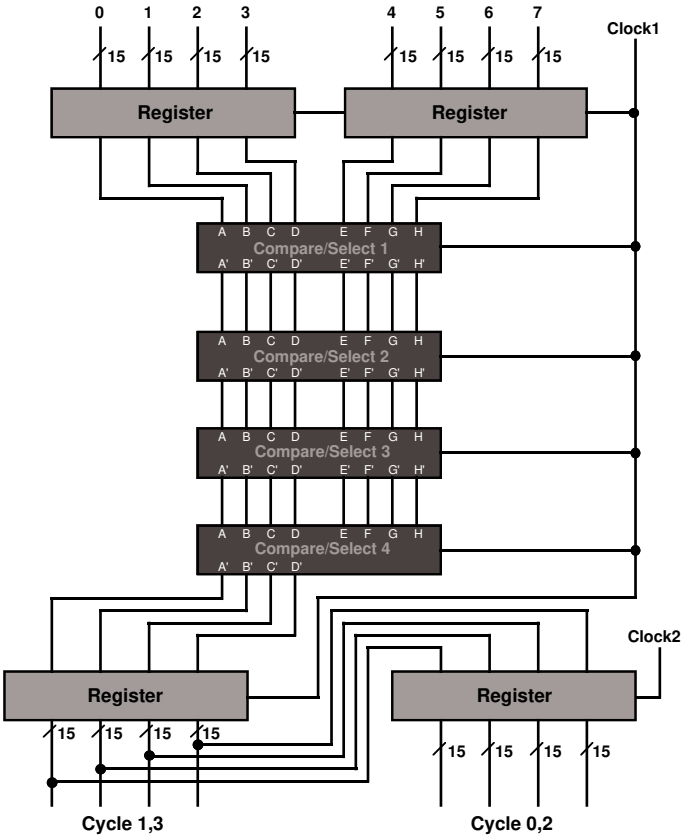

Figure 20. Sort ASIC MAX4 block diagram.

During the next three 6.25 nsec clock cycles the data is passed through the remaining three Compare/Select circuits. Only the left four operands are stored at the end as they contain the four maximum of the original eight operands. One clock cycle later the first results are stored in the register shown at the bottom right. The register to the left now contains the four largest values from the second set of eight operands. These two sets of four operands must be examined to select the four largest among them. This second level of selection occurs in the second MAX4 block shown near the bottom of figure 18. During the next two 6.25 nsec cycles the last two sets of four maxima are generated in the top MAX4 circuit and passed on, through

the 2:1 multiplexer, to the second MAX4 circuit. New data enters the second circuit every 12.5 nsec. This circuit is clocked at 160 MHz, but the data is interleaved with empty cycles.

After four more 6.25 nsec cycles, the four maxima from the first sixteen operands are at the Cycle 1,3 outputs of the second MAX4 circuit. This result is clocked into the Cycle 0,2 register of the circuit before it is overwritten by the empty cycle immediately following. The second register is clocked with an 80 MHz clock instead of the 160 MHz clock. Thus the first result is held for 12.5 nsec providing enough time for the empty cycle to clear and the maximum 4 from the second 16 operands to be clocked in. These eight values are presented back to the inputs of the second MAX4 circuit through the right side of the 2:1 multiplexer during one of the empty cycles. They are interleaved with new data from a later crossing. Thus, the four largest of the original 32 operands finally appear at the bottom of the second MAX4 circuit approximately 4 crossings (100 nsec) after the data first entered the Sort ASIC. This result is captured in the register as shown at the bottom of Figure 18. This register is clocked at 40 MHz making the results available at the outputs of the ASIC for a period of time equal to a full crossing (25 nsec). The latency for the full sort operation without any optimization is four crossing times, or 100 nsec.

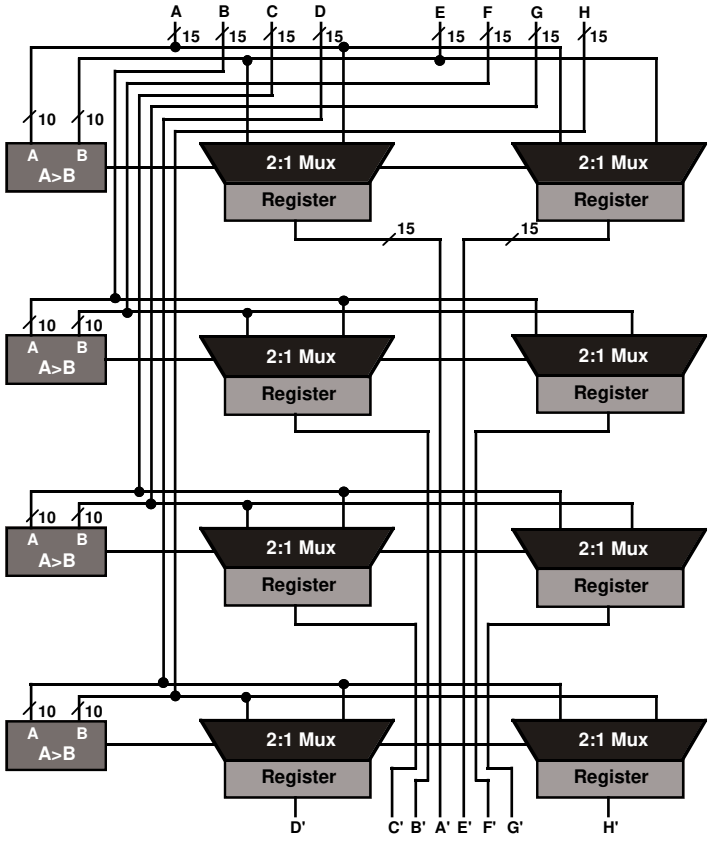

Figure 21. Sort ASIC Compare/Select block.

5.4.1.3 Boundary Scan

We intend to implement the same controller and instruction decoder for boundary scan as used in the Adder and Isolation ASICs. All ASICs in the Level 1 trigger processor will have compatible boundary scan circuits.

5.5 Outputs

Each Electron Isolation card produces four ranked trigger category values (6 bits in length) each combined with a single bit indicating which of the two 4 x 4 regions produced the value. These results are produced once every 25 nsec crossing. Every 6.25 nsec one of the values is placed on the backplanes using a set of 7 differential pairs. All four values are transmitted to the Jet Summary card during the period of one crossing. These 14 lines, together with the 304 input lines noted above, use 318 pins on the 340 pin connector. Additional pins will be used for clock, controls, and status information.

6. Jet Summary Card

The Jet Summary card sits near the middle of the trigger data processing section of each regional trigger processing crate. It is shown in Figure 3 situated in the front portion of the crate between the 4th and 5th Electron Isolation cards. It collects and summarizes data from both the Receiver cards and the Electron Isolation cards at 160 MHz. The Jet Summary card has the same form factor as the Electron Isolation card, 9U x 280mm. It has a VME interface via a 128 pin, 4 row DIN connector. The trigger data is received on an AMP 340 pin connector.

The electron trigger rank information from eight Electron Isolation cards (32 values) is sorted to produce the four highest ranked electron triggers. These values have a 4-bit address appended to them which indicates which 4 x 4 trigger tower region, covered by the crate, produced them. The E_T information from the Receiver cards is also on a 4 x 4 tower resolution. These values are summed by a pair of Adder ASICs to produce a total E_T sum. The same information is processed by a Sort ASIC to determine the four largest E_T values produced by the crate. This is used as the jet trigger. In addition, we test the E_T in 4 x 4 tower regions against a series of thresholds and encode the results in 4 bits. The E_T information from the Receiver card is also sent to memory lookup tables which generate E_X and E_Y for each 4 x 4 region. The E_X and E_Y values are summed individually in the Adder ASICs to produce total E_X and E_Y for the 256 tower region of the calorimeter covered by the crate.

The Jet Summary card also contains logic to search for tau candidates by testing for isolated hadrons. This logic will be based on the existing E_T sums

in 0.35 eta x 0.35 phi regions and the isolated electrons that are already present on the card. One of the tests that can be implemented is to determine if a high fraction of the total observed E_t in the 0.35 x 0.35 region is contained in a single trigger tower. Such regions are candidates for isolated hadrons. Another test is an extension of the electron/photon algorithm and exploits the fact that the tau hadronic jet is characterized by a local e.m. energy deposit. Other algorithms are being studied and space for the implementation of such algorithms is reserved on the card.

Space has also been allocated for the luminosity algorithm described in section 1.6. This circuit may be moved to the global trigger processor, but until this design decision is determined we reserve the space on the Jet Summary card.

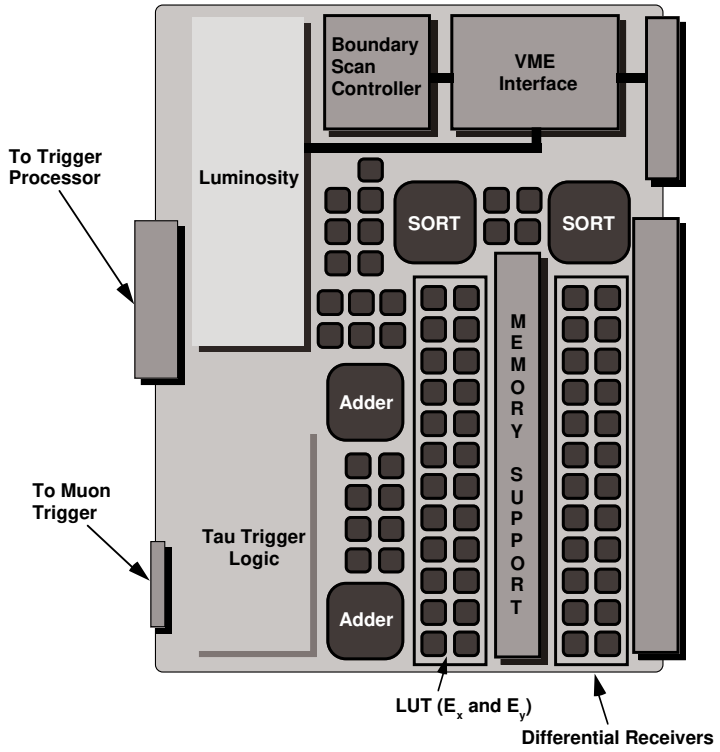

Figure 22. Jet Summary card.

6.1 Inputs

Each of the eight Electron Isolation cards transmits 6 bits of trigger rank every 6.25 nsec in differential mode. A single bit indicating which of the two 4 x 4 trigger tower regions generated each rank is also included. Therefore, the Jet Summary card receives 7 differential pairs from each Electron Isolation card for a total of 112 input pins.

The Receiver cards send the 13 bits of E_T information for the two 4 x 4 trigger tower regions differentially on 26 lines. This data is transmitted at 160 MHz, requiring two 6.25 nsec time frames. The third 6.25 nsec time frame contains

the Quiet and Minimum Ionization information for the two 4 x 4 regions. The remaining bits in the third and fourth 6.25 nsec time frames are at present reserved for future assignment. The Jet Summary card receives this data from the eight Receiver cards on 208 input pins. Therefore, the total number of signal pins dedicated to trigger data is 320.

6.2 Outputs

The outputs from the Jet Summary card appear on connectors at the front edge of the card. Transmission is via twisted pair cable at 40 MHz. Two connectors are shown in Figure 22, but the top connector to the global trigger processor is likely to be split into several separate connectors to segregate the individual quantities. The bottom connector is for the Muon Trigger and contains a Quiet region map of 16 bits (one bit per 4 x 4 region).

The global trigger processor receives 10 bits of E_T , 13 bits each of E_X and E_Y , 40 bits for the top 4 Jets, 24 bits of electron trigger rank, 4 bits of Jet E_T threshold information, 16 bits of location for the top 4 electrons, and 16 bits of information for the top 4 jets.

7. Latency

The overall latency of the level 1 calorimeter trigger regional logic design described in this document is approximately 13 crossings, or 325 nsec. This latency follows a latency of 4 crossings after the interaction for the physics signals to propagate to the calorimeter readout, 13 crossings for processing by the calorimeter front end electronics, 30 crossings to account for the maximum possible fiber optic cable length of 150 m for transmission of the data from the front end electronics to the calorimeter trigger logic in the electronics barracks and another crossing for synchronization of the data to the regional calorimeter trigger. We estimate that the transmission of the output of the regional logic information to the global calorimeter trigger logic will take another 4 crossings (including one crossing for synchronization). The result is that the calorimeter trigger information is provided at the input of the global calorimeter trigger approximately 79 crossings after the interaction occurred.

The 13 crossing latency of the regional calorimeter trigger logic is divided amongst several stages. Since the logic is mostly clocked at 160 MHz, the operations are composed of 6.25 nsec cycles, four of which add up to a single 25 nsec crossing time. The Receiver card uses 1.5 crossings after the synchronization stage divided into two 6.25 nsec cycles and a full crossing to accommodate crate to crate data transfers. The first 6.25 nsec cycle is used for the memory lookup table and the second is used to stage the information to the output connector. The data transmission across the backplane from the Receiver card to the Electron Isolation Card uses a single 6.25 nsec cycle.

The longest latency operation performed by the regional calorimeter trigger logic is that of the isolated electron identification and sort. Other data will be held in memory to wait to be aligned with these results. We therefore examine this function to determine the overall latency.

The Electron Isolation Card used 5.75 crossings to find and sort the isolated electrons. Most of this time is spent in the sort operation. The Isolation ASIC is fully pipelined and therefore is able to accept a new crossing's worth of data every 25 nsec. However, its overall latency is 1.5 crossings (37.5 nsec). The first 3 6.25 nsec cycles are used for the first 3 stages of the Isolation ASIC logic. The fourth cycle is used for the 4-way compare and the last 2 cycles are used to set up and place the results at the output stage for the Sort ASIC. The Sort ASIC then finds the 4 highest rank candidates of the 32 inputs in 4 crossings, accepting 32 new candidates every crossing. One more 6.25 nsec cycle is then used to stage the results to the output connector.

The transmission of the 4 highest rank electron candidates on the backplane from the Electron Isolation card to the Jet Summary card takes one 6.25 nsec cycle. The Jet summary card then sorts its total of 32 input electrons from 8 Electron Isolation cards through another Sort ASIC with a 4 crossing latency and uses another two 6.25 nsec cycles to stage and present the Crate's four highest rank electron candidates on the cable for transmission to the global calorimeter trigger. The total from Receiver card synchronization to output of the Jet Summary card is 12.25 crossings or slightly more than 306 nsec. We retain some additional time as contingency and give the Regional Calorimeter trigger latency as 325 nsec.

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