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RECONFIGURABLE HARDWARE APPROACH TO BUILD THE CENTRAL TRIGGER PROCESSOR

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1. Introduction

The current status of the Central Trigger Processor (CTP) development [1] does not cover very much the structure of its control part and the format of the control data. The general layout of CTP [2] does not include the control logic and control busses. Nevertheless, everybody knows that this part will require significant amount of hardware.

Investigation of the CTP critical components showed that FPGA devices could be considered as good candidates for final implementation of the CTP architecture. The most difficulty may occure in FPGA implementation of Look-Up Table (LUT) and especially in having access to the internal memory blocks available in the XILINX devices of 4000 series to store the individual reference patterns corresponding to the selection criteria for each Sub-Detectorn Pattern (SDP) of the CTP. Currently this option does not supported by the design tools for VHDL input feature.

Generally FPGA devices contain the special interface for downloading the configuration data which finally determins the exact internal hardware architecture and interface to the outside signals. Usually the time, required for the configuration process, does not exceed several milliseconds, depending on the protocol.

Many applications are based on the idea of reconfigurable hardware [3], [4].

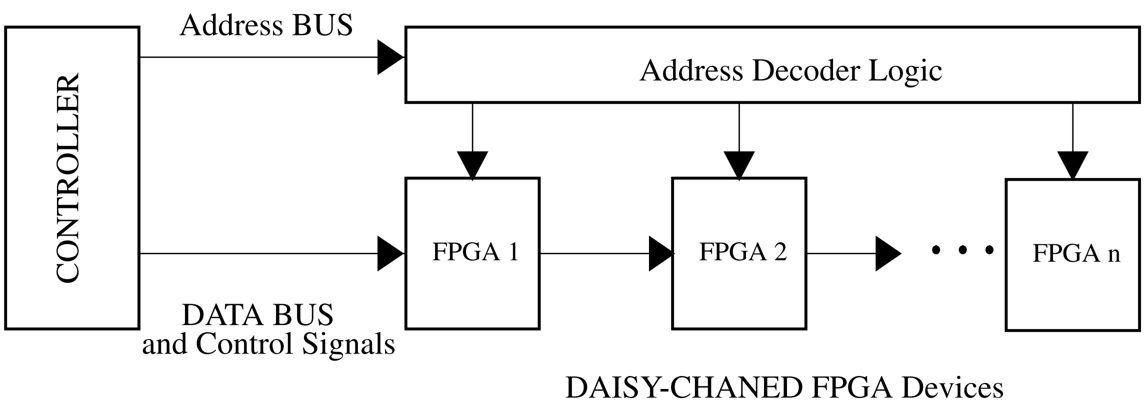
Amtel AT6005 is a fine-graned FPGA which is presently the only commercially available device capable of being dynamically reconfigured, i.e. selectively reconfigured while the logic array is active. It might be foreseen that in its major parts CTP does not require to be reconfigured dynamically. Therefore the popular XILINX FPGAs may be used to build the CTP basing on the proposed approach.

2. FPGAs as Reconfigurable Hardware Units

Configurable Logic Block (CLB) as the main element of logic array contains two Functional Generators (FG) which are actually implemented as a simple 16x1 LUT and may therefore perform any logic function (eg. AND on Fig.2).

The content of FG's configuration memory is combined with the other configuration information for each CLB, Input-Output Block (IOB) and routing into a big frame of configuration data. The error check coding is also included into the frame. During several milliseconds it could be than downloaded into the daisy-chained FPGA devices (Fig.1) using the special protocol.

Figure 1. Asynchronous Periferial Mode for loading configuration data into FPGA devices.

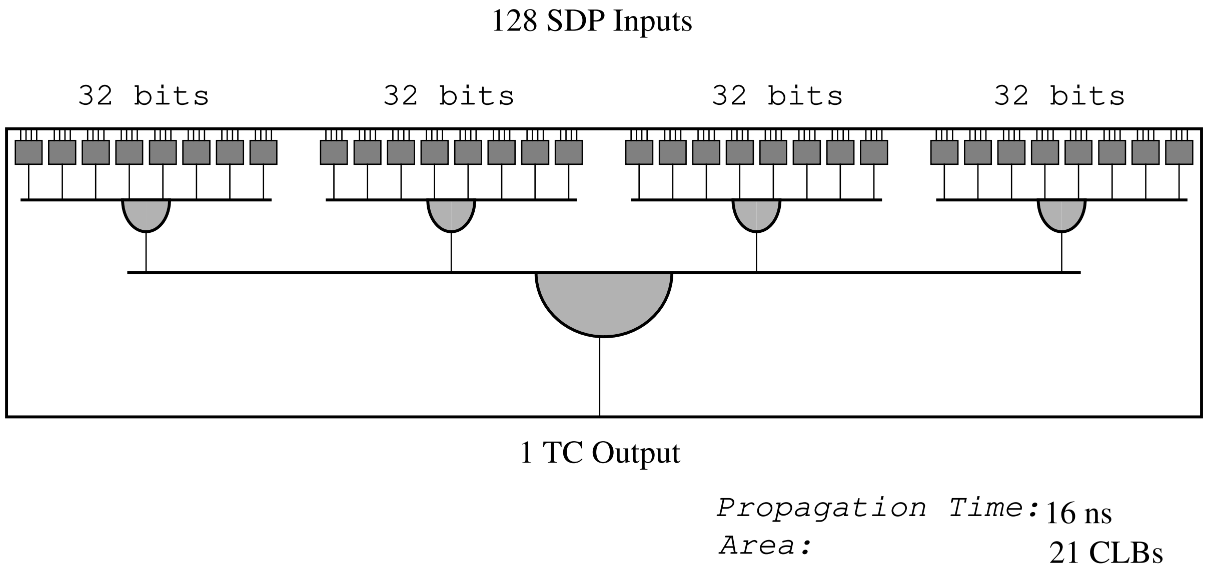


The reconfiguration process of the FPGA's internal hardware architecture is similar to the control function in conventional electronics design. Therefore, each FPGA device contain all necessary logic to support the control features. Additionally it maintains the verification (READBACK) and testing (BOUNDARY SCAN) options.

3. Reconfigurable Hardware Solution for LUT

The proposed LUT configuration for FPGA implementation (Fig.2) includes the definite number of FGs, connected together into 128 bits wide word to make the common 1 bit solution for each Trigger Candidate (TC). After being loaded, each FG performs it's own logic function and this structure can be considered as a usual 128 to 1 decoder.

Figure 2. Possible Solution for the LUT Implementation in FPGA
(XILINX 4K)



There are several possible ways to change the logic function for individual TC. Although XILINX 4K devices allow an access to the memory of each FG, only schematic input with hard macros library can be used now. It is possible to use the input TC description table for VHDL design flow. In the both cases the reconfiguration process may take several hours.

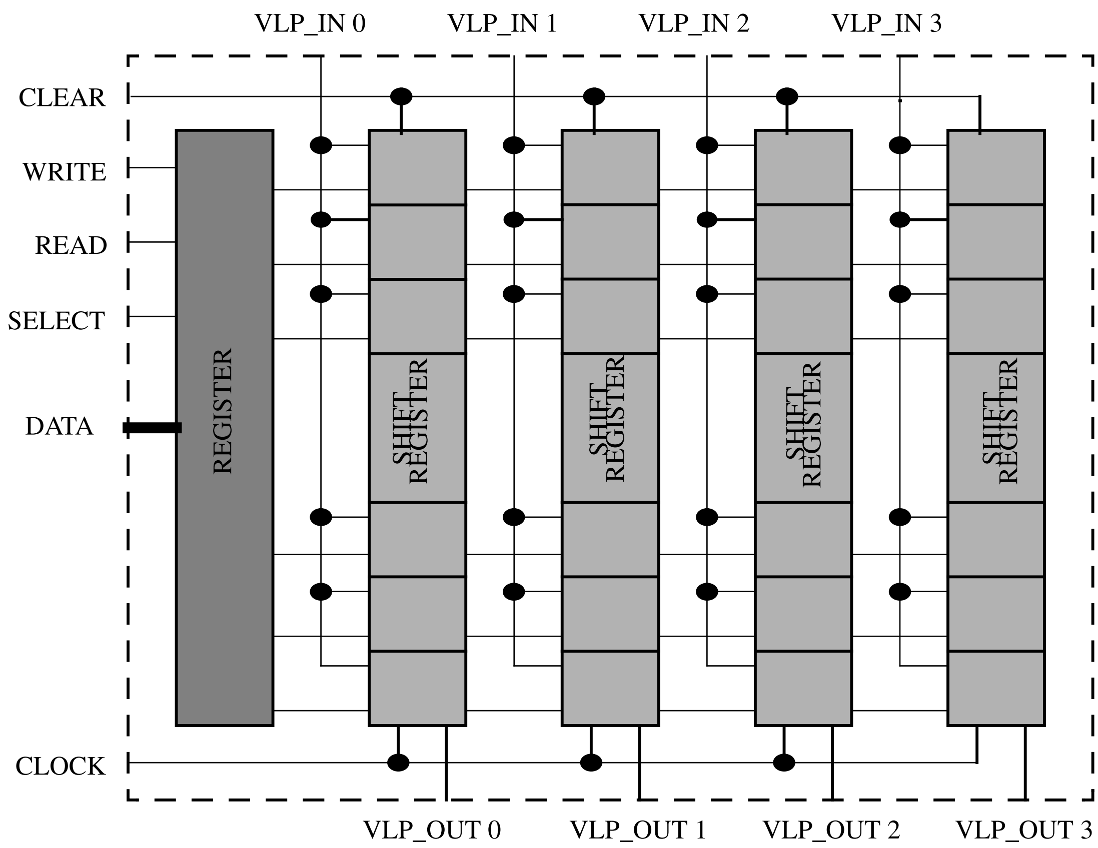
The dedicated software tool is required to allow the translation from input table with TC reference patterns into loadable framed format for configuration stream.

4. Critical Components

We can extend this approach to other critical components of the CTP. Let us consider, for example, Variable Length Pipline (VLP) (Fig.3). The control logic with associated parts occupies approximately 30% of the whole logic amount for the shown example with 4 bit SDP partitioning. It is possible to build shift registers of individual length for each bit of SDP or any group of bits as a pure sequence of flip-flops using a Reconfigurable Hardware approach. It will save additional space and increase the speed of given component at least twice.

In case of Prescaler we can save more than 50% of space without significant increase in speed. Additional resources may be allocated by creating prescalers of individual size depending on the prescaler factor. It is not likely that the prescale factor for the majority of TCs will be close to 4000 that requires 12 bit prescalers.

Figure 3. VLP Layout



For each critical component of the given size the prerouted and well optimized macros can be created. The dedicated software package will allocate components according to the supplied CTP configuration, place them as predefined macros and connect together and to the IOBs to make an external interface which will be defined by the interconnection between FPGAs on the PCB. The produced configuration stream after being downloaded into CTP hardware will define the exact architecture corresponding to the CTP configuration parameters.

5. The Advantages of Reconfigurable Hardware

Besides the advantages of saving the logic amount and increasing the operation speed for some components, due to the fine partitioning as a result of the given approach, there are some other opportunities to improve the functionality and flexibility of the CTP.

1. We can drastically decrease the number of control lines and use the spare IOBs for data flow means.

2. Monitoring resources (scalers, etc.) could be reallocated according to the current needs during the test period. We can work with the reasonably reduced resources of monitoring hardware and do not insert scalers in every point of the CTP to presume the possible future needs.

3. By downloading the test architectures on place of some CTP components we can test

other parts of the CTP itself and its PCB(s), Monitoring System and interface to Level 2 Trigger System. As an example, instead of multiplexing data from VLP and Random Pattern Generator (RPG) used in some testing options [2], it is possible to reallocate the space, normally occupied by VLP, to RPG structure.

6. Device Overview

Another similar to XILINX FPGA architecture is offered by AT&T. Their Optimized Reconfigurable Cell Arrays (ORCA) devices have the average speed characteristics approximately 25% better than ones from XILINX. Additionally, AT&T produces the significantly larger arrays with the different structure of Programmable Logic Cell and enhanced flexibility. The comparison between theese two series of products is given into Tab.1.

Table 1:

Device	Usable Gates	Flip-Flops	Max. RAM Bits	User I/Os	Array Size	Vendor
XC4010	10,000	1,120	12,800	160	20 x 20	XILINX
XC4013	13,000	1,536	18,432	192	24 x 24	XILINX
XC4025	25,000	2,560	32,768	256	32 x 32	XILINX
2C15	15,000	1,600	25,600	320	20 x 20	AT&T
2C26	26,000	2,304	36,864	384	24 x 24	AT&T
2C40	40,000	3,600	57,600	480	30 x 30	AT&T

7. Conclusions

Some software research will be needed to produce the specialized tool for effective and fast translation of the list with CTP parameters into the configuration flow for CTP hardware.

The new FPGA devices with attractive characteristics are commercially available now.

Acknowledgement

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References

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