Bunch-Crossing Identification for the ATLAS First-Level Calorimeter Trigger

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ABSTRACT

As part of the design studies for the ATLAS first-level calorimeter trigger, we have been investigating the process of bunch-crossing identification (BCID). Various digital BCID algorithms have been investigated using software simulation. Furthermore, a demonstrator system has been constructed which performs BCID on 36 channels of trigger data. The BCID algorithms are implemented in Field-Programmable Gate Arrays (FPGAs). The field-programmable nature of the system has allowed a number of BCID algorithms to be tested in a CERN test beam. The initial results show BCID being performed with good efficiency on signals corresponding to energies of a few GeV. An ASIC which performs BCID has been designed, built and tested in a CERN test beam.

INTRODUCTION

At the Large Hadron Collider (LHC) the bunch crossing rate is 40 MHz (one crossing every 25 ns). With the exception of the tile calorimeter, the calorimeters proposed for ATLAS [1], are intrinsically slow and produce output signals which extend over several 25 ns periods. For the first-level trigger these long pulses present a problem which has to be solved in real time. The problem is two-fold. Firstly, the LHC bunch crossing responsible for the energy deposition that produced the pulse has to be identified, and secondly a measure of the energy deposition has to be extracted. This operation is essential to avoid spurious trigger generation or trigger suppression by out-of-time data samples. The work described in this paper has so far concentrated primarily on techniques to establish the correct timing of pulses.

The first-level calorimeter trigger for ATLAS is based on a digital processor [2]. The pulse heights of the calorimeter signals are measured every 25 ns by a system of FADCs. The function of the bunch-crossing identification logic is to determine, for each calorimeter pulse, the digitised value which corresponds to the pulse peak, pass this on to the digital processor and set all other digitisings to zero. Figure 1 illustrates this process.

As part of our studies into the ATLAS level-one calorimeter trigger, we have been investigating various ways of implementing a digital BCID algorithm [3]. Extensive software simulations have been performed for a number of algorithms and a hardware demonstrator has been constructed which has allowed BCID logic to be tested in real time in a CERN test beam.

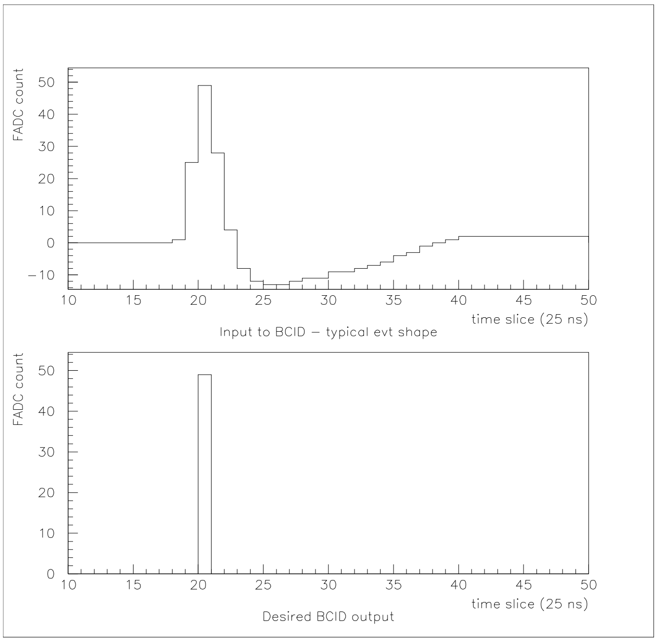

Figure 1: Ideal BCID Output

BCID ALGORITHMS

Any candidate BCID algorithm must meet two requirements. Firstly, it must be efficient for calorimeter pulses of all sizes: BCID becomes harder to perform with good efficiency for both small pulses, where the signal-to-noise ratio is decreased, and for large pulses, specifically those which are sufficiently large to saturate the FADCs. In this latter case the pulses observed will no longer match the characteristic shape expected from the front-end shaping electronics. Secondly, the algorithm must be simple, so that the contribution which the process of BCID makes to the total latency of the level-one calorimeter trigger is kept to a minimum.

A variety of digital algorithms have been studied. For example:

- Peak Finder
- Deconvolution Filter
- Zero-Crossing Identifier
- Constant-Fraction Discriminator

Of these, the peak-finding algorithm is the simplest: three consecutive samples are examined by a pair of comparators, which search for peaks in the data. If a peak is found, that data sample is passed on to the trigger processor. If a sample does not correspond to a peak, the datum in that sample is zeroed before being passed on to the trigger processor.

The other algorithms listed above are all standard methods of extracting timing information from a pulse and are described elsewhere [4]. It should be noted however, that when implemented as digital algorithms, all of the above can be performed using two simple processes: a finite impulse response (FIR) filter and the peak-finding algorithm described above.

Figure 2: The Structure of the BCID algorithm

Figure 2 shows the structure of such a generic BCID algorithm. The 8-bit digitised pulse heights are stored in a pipeline memory while the BCID algorithm is performed. The FIR filter extracts samples from this pipeline memory and convolves them with a given set of coefficients. The purpose of the FIR filter is to reshape the pulse, producing a peak which is less susceptible to corruption due to noise or FADC saturation than that of the original pulse shape. The filtered data is written into a second pipeline memory, the contents of which are examined by the peak finder. The decision produced by the peak finder is used to gate the output from the original pipeline memory to the calorimeter trigger processor.

BCID SIMULATION STUDIES

Extensive software simulation studies have been used to evaluate the performance of a range of digital BCID algorithms. The algorithms were simulated in FORTRAN and tested off-line with real calorimeter data. The data were recorded at a CERN test beam using the ATLAS first-level trigger demonstrator system [5] connected to the RD3 prototype of the ATLAS barrel calorimeter.

Data were recorded with a wide variety of beam conditions, including pions and electrons at a range of energies, from 10 to 300 GeV. The calibration of the FADCs used to digitise the data was 1 GeV/count. The pulses sat on a pedestal which had a typical height of 26 counts and an RMS width of 0.5 counts.

Simulation Results

The table below shows some of the results from the BCID simulation studies.

BCID Algorithm	Pulse Height Above Which 100% Efficiency Is Achieved
Peak-Finder ($S_{n-1}<S_n\geq S_{n+1}$)	4 Counts
Zero-Crossing Identification.	7 Counts
Constant Fraction Discriminator.	4 Counts
Peak-Sharpening algorithm (FIR coeffs.= –1, 0, 4, 0,–1)	3 Counts

These results were obtained from a study of around 300 events per pulse height. For pulses which had a height of greater than 7 counts (7 GeV) all of the algorithms performed with 100% efficiency. Below this it can be noted that the peak finder – the simplest of all the algorithms tested – gave results comparable to the best of the more complex algorithms. From these results it was concluded that BCID could be performed with good efficiency using relatively simple algorithms.

The BCID Demonstrator System

Tests of a single-channel BCID prototype were made at CERN in 1992 [6]. For the present studies, a more compact demonstrator system has been constructed which performs BCID on 36 channels of calorimeter trigger data. The BCID logic is implemented in Xilinx Field-Programmable Gate Arrays (FPGAs). The re-programmable nature of these devices allows the system to perform a variety of BCID algorithms. It has been tested in a CERN test beam as part of the ATLAS first-level trigger demonstrator system [5]. Figure 3 shows the complete system.

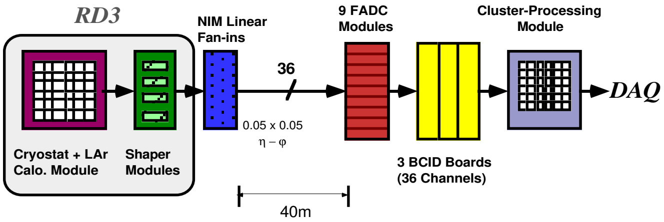

Figure 3: The First-Level Calorimeter Trigger Demonstrator System.

The demonstrator system processes a 6 × 6 area of trigger cells. A trigger cell granularity equivalent to $\Delta\eta \times \Delta\phi = 0.05 \times 0.05$ in the ATLAS barrel is acheived by the use of commercial linear fan-in modules to sum the analogue signals from the calorimeter shaping modules. The summed signals are then transmitted down 40 m long BNC coaxial cables to the first-level trigger demonstrator system. They are digitised by FADCs [7] using a free-running 40 MHz clock and a TDC is used to record the phase of this clock relative to the time of arrival of the test beam particle. During off-line data analysis the TDC measurement is used to veto any data where the calorimeter pulse is sampled more than 3 ns away from its peak. This off-line cut replicates the situation that will be present at the LHC, where the sampling process is phase-locked to the bunch-crossings.

After digitisation, the resultant 36 channels of 8-bit data are passed to the BCID system. The BCID system consists of three boards, each processing 12 channels of data. The first task which is performed by each BCID board is pedestal subtraction – the pedestals upon which the calorimeter pulses sit are removed by means of a look-up table. The BCID algorithms themselves are implemented inside FPGAs (XC4008 devices), each of which process four channels of calorimeter data in parallel. Which BCID algorithm the FPGAs implement is determined by the design file with which they are configured. The design files are downloaded into the FPGAs from the VME-based data acquisition (DAQ) system. Based on the results of the previous software simulations, design files have been created for eleven different BCID algorithms.

After BCID has been performed, the 36 channels of data are transferred via the crate backplane to the Cluster Processing Module (CPM). This module implements the e/γ cluster-finding algorithm which will be employed by the ATLAS first-level calorimeter trigger [5]. The effect of BCID on this cluster-finding process can therefore be studied in real-time.

The data appearing at various points in the trigger system are read out and recorded using an Exabyte storage system. Data are read out from memories positioned at the output of the FADC board, the input and output of the BCID board, and the input and output of the CPM.

Test Beam Results

The 36-channel BCID system was first tested in CERN test beam in June 1995. The calorimeter used was the RD3 prototype of the liquid argon accordion barrel calorimeter. Data were taken with electron and pion beams, with beam energies from 20 GeV to 300 GeV. Data were recorded with a range of different front-end electronics, which produced analogue pulses with a variety of different shapes

So far, most of the analysis performed on the data recorded at this test beam has been conducted to search for faults in the hardware. Only minor faults have been discovered and in general the system behaves as expected. Analysis is currently being conducted to evaluate the performance of the BCID system.

Figure 4 shows the system performing BCID on a real calorimeter pulse, produced by a 50 GeV electron. The pulse was recorded at the input and at the output of the BCID board. It can be seen that the pedestal of 30 counts height has been removed, and BCID has been performed: only the peak of the pulse has been gated through the system. The BCID algorithm used here is the peak finder. It can be seen from the relative position of the peak in the two plots that, when implemented inside the FPGA, the algorithm has a latency of eight clock cycles.

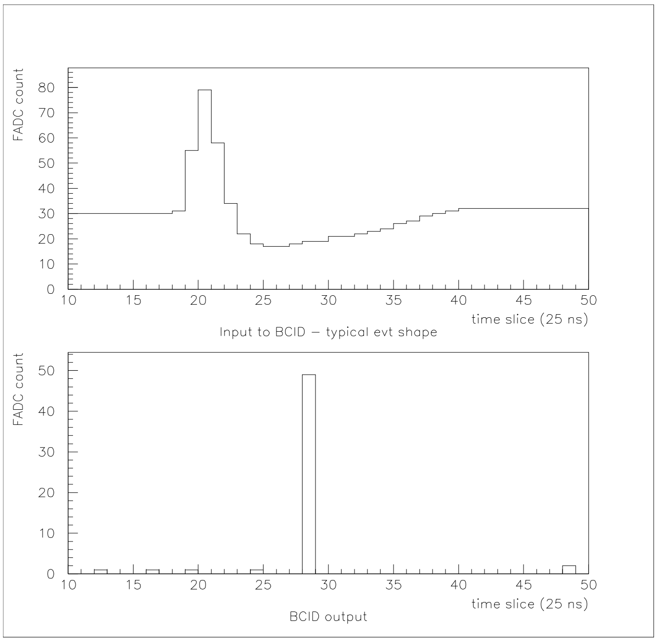

Figure 4: BCID on a Real Pulse.
BCID Algorithm =_Peak Finder $(S_{n-1}<S_n\geq S_{n+1})$.

Figure 5 shows the efficiency of the peak finder algorithm as a function of pulse height. The horizontal axis shows the peak height of the pulse in GeV, whilst the vertical axis shows the percentage of pulses at that height for which BCID was performed correctly. This plot is based upon around 500 events, distributed evenly over the energy range, so these results should be regarded as preliminary.

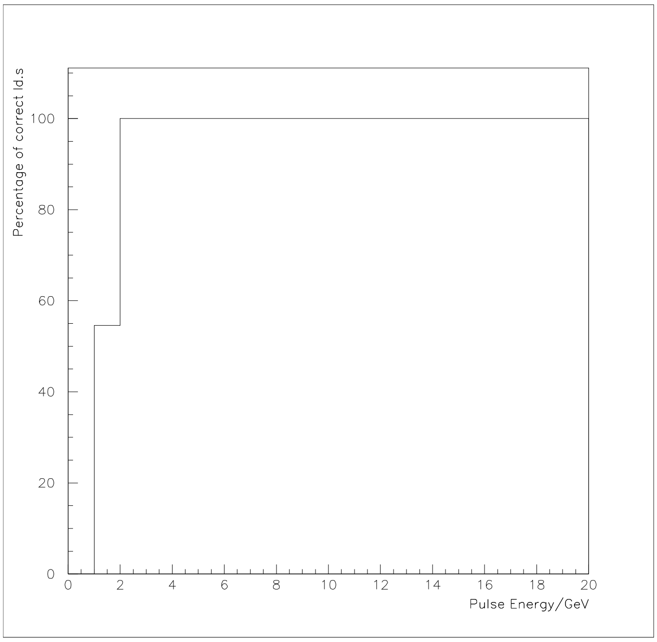

Figure 5: Efficiency of BCID as a Function of Pulse Height.
BCID algorithm = peak finder ($S_{n-1}<S_n\geq S_{n+1}$).

Initial results show BCID being performed with good efficiency for pulses down to a few GeV. Analysis of the test beam data is continuing. The demonstrator system is currently back in a CERN test beam, collecting more data.

THE BCID ASIC PROGRAMME

There are several disadvantages in using FPGAs to perform BCID for the ATLAS first-level calorimeter trigger. FPGAs are large and expensive and, when implemented in FPGAs, the BCID algorithms have a greater latency than is desired for the final system. It is therefore planned to use ASICs in the final BCID system.

As a move towards this, one of the algorithms tested has been converted into an ASIC design. To develop this, Verilog HDL was used for the behavioural description of the BCID design. The chip layout was synthesised using the ES2 Standard Cell Library and the chip was manufactured by ES2 in 1.0 µm technology [8].

An adapter board has been designed and built which maps the pinout of the BCID ASIC on to the FPGA sockets in the BCID demonstrator system. Data have been taken in the current CERN test beam with the BCID ASICs installed in the demonstrator system. Detailed analysis of the data recorded is underway, but preliminary results indicate that the ASIC performs correctly and with lower latency than the FPGA.

CONCLUSION

Bunch-crossing identification is an essential part of the first-level calorimeter trigger. Software simulation has shown that BCID can be performed with good efficiency using relatively simple algorithms. In our hardware demonstrator programme we have shown that these algorithms can be implemented in FPGA or ASIC technology, running at the required frequency.

ACKNOWLEDGEMENTS

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