A first-level calorimeter trigger for the ATLAS experiment

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ABSTRACT

In the RD27 collaboration we have carried out system studies on the implementation of a first level calorimeter trigger processor system for the ATLAS experiment. These system studies have led to the design of a fully synchronous calorimeter trigger processor system using commercial high-speed optical links. The links will terminate in multi-chip modules incorporating custom-designed integrated optics, and the trigger algorithms will be implemented in ASICs.

The full system can be contained in six 18SU size crates which will process approximately 4000 electromagnetic and 4000 hadronic trigger cells and provide the central trigger processor with signals from events with high-P_T electrons/photons, jets and missing-E_T.

SUMMARY

The following is a summary of the work carried out by the UK group within the RD 27 collaboration. An alternative system architecture is pursued by a Swedish group (C. Bohm et.al.,) within the same collaboration.

The calorimeter trigger must select events on the basis of electromagnetic (e.m.) clusters produced by electrons or photons, jets, and missing transverse energy. Our development efforts have focused on e.m. cluster trigger logic, since this presents the biggest rate problem and is the most challenging component of the trigger system.

In the first phase of our work, an ASIC (RAL114) was designed and tested which implemented an electromagnetic cluster-finding algorithm. Each ASIC carried out the algorithm for one trigger cell. Using this modularity, the final system would need approximately 50 18SU-high crates. We have therefore studied how to process 16 trigger cells in each ASIC. Our studies show that the number of crates needed for the entire processor could then be as few as six. The ASIC will require 8-bit data from 49 e.m. and 49 hadronic cells, which is impractical in parallel format, but if data are serialised then the ASIC will need only one pin per trigger cell. The bunch-crossing rate at LHC will be 40 MHz, so to send 8-bit data in serial format from the ADC system requires a data rate to the ASIC of up to 320 Mbit/s per pin per trigger cell. This is not yet possible with semi-custom CMOS technology, so we are pursuing a 160 Mbit/s two pin per trigger cell solution.

In conjunction with industrial partners, a Multi Chip Module (MCM) containing integrated optical devices with fibre pigtails attached will be developed to receive the optical signals from the ADC system at 800 MBaud (including coding) from two trigger cells. Each MCM will handle data from eight trigger channels. A single channel of the MCM will contain an integrated optical device, which will carry out the optical to electrical conversion, a serial to parallel converter to translate the incoming serial bit-stream to a 16-bit word every 25 ns, and a custom ASIC (RAL163) which will convert the two 8 bit words into four serial links operating at 160 Mbit/s.

The MCM will be evaluated in a demonstrator system in a test-beam during 1996.

REFERENCE

[1] V. Perera et al., A First-Level Calorimeter Trigger Processor for The Large Hadron Collider, IEEE Transactions On Nuclear Science, Vol. 40, No.4, August 1993.

[2] V. Perera et al., A First-Level Calorimeter Trigger for the ATLAS experiment, IEEE 1994 Nuclear Science Symposium and medical Imaging Conference, Norfolk, Virginia, October 30 - November 5, 1994.