A test of the ATLAS First Level Muon Trigger logic

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ABSTRACT

We present the design of the first level muon trigger in the central toroid of the ATLAS experiment at the Large Hadron Collider (LHC). The trigger [1] is based on fast, finely segmented gaseous detector, Resistive Plate Chambers (RPC), to unambigously identify the interaction bunch crossing and to provide a sharp threshold over a large interval of transverse momentum. We describe the logic scheme of the trigger and the performance of a circuit prototype tested on a beam.

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1. Introduction

Experiments at high energy, high luminosity hadron colliders will need flexible inclusive lepton triggers to select a variety of processes of primary interest for studying the production of Higgs bosons, of supersymmetric particles and the phenomenology of the top quark. The high bunch crossing frequency and the high radiation level at the LHC are the main constraints for the design of the first level trigger.

The proposal of using a fast, finely segmented, detector dedicated to implement the first level muon trigger was first presented in 1990 [2]. This simple trigger scheme exploits the fast response of RPC [3] and their low sensitivity to low energy photon and neutron background [4][5]. Other advantages of RPC are the low cost of mass production and the flexibility in segmentation that makes their use attractive in different spectrometer configurations. In fact this trigger scheme has been adopted by both pp experiments at the LHC [6][7]. Beside the need for a very good time resolution, another requirement for use at the LHC is full efficiency at high rate. Good progress has been made during the last years to achieve the required performance [8] [9] and more recent results have been presented at this conference.

The ATLAS muon spectrometer design emphasises reliable, high-resolution, standalone performance over a p_T range from 5 to about 1000 GeV/c. Precision momentum measurement and triggering are done by two dedicated detectors: Muon Drift Tubes (MDT) and RPC. The trigger chambers also provide the second coordinate measurement and timing information to relate muon tracks to bunch crossings of period $T = 25\ ns$. The low-energy charged and neutral particles flux at the LHC will be fairly high [10]. These backgrounds have a major impact on the trigger rate and pattern recognition efficiency.

2. Trigger system

The transverse momentum selection is done with a fast coincidence between strips on different planes. The number of trigger planes is defined by the need to minimize the rate of accidental coincidences and to optimize the efficiency. To reduce the accidental rate to a level lower than the prompt muon rate, the trigger will operate in two projections,

$r-z$ and $r-\phi$. The trigger detectors will also be used to provide the coordinate in the non-bending plane $(r-\phi)$ to the muon tracking system. The different momentum selection criteria required by the relevant

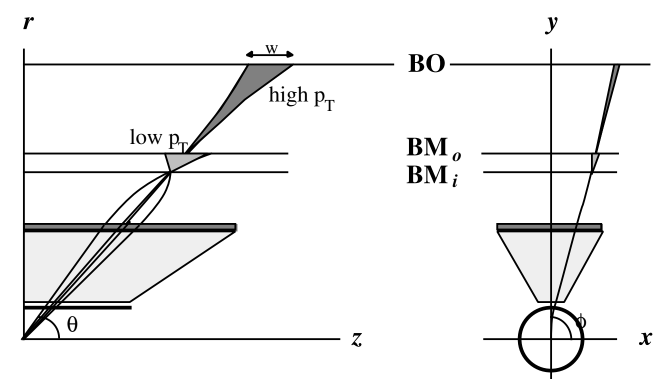

Figure 1: Scheme of the first-level muon trigger in the barrel

physics processes are best met using a *low* and a $high-p_T$ trigger. This is implemented in the barrel as shown in Fig.1. The trigger scheme uses three stations, two middle stations (BM), each made of two RPC planes and the outer station (BO), made of three RPC planes.

Each RPC plane will be equipped with read-out strips on either side of the gas volume: z-strips parallel to the magnetic field and ϕ-strips parallel to the beam.

The size of the trigger window, to select muons with transverse momentum larger than p_T is $w \simeq a/p_T \sin^2\Theta$, where p_T is the value of the transverse momentum after traversing the calorimeter. Fluctuations in the energy loss and multiple scattering in the calorimeter, lenght of the interaction region and non uniformity of the magnetic field are all smearing effects which make the choice of $3-4\ cm$ strip pitch a balanced choice between good selectivity and number of channels.

The $low-p_T$ trigger requires a three-fold majority of the four BM planes while the $high-p_T$ trigger requires a two-fold majority of the three BO planes in coincidence with the $low-p_T$ trigger. The trigger rate in the barrel is shown in Fig.2 as a function of the luminosity for the low-p_T ($p_T > 5\ GeV/c$) and high-p_T ($p_T > 20\ GeV/c$) trigger configurations together with the prompt muon rate.

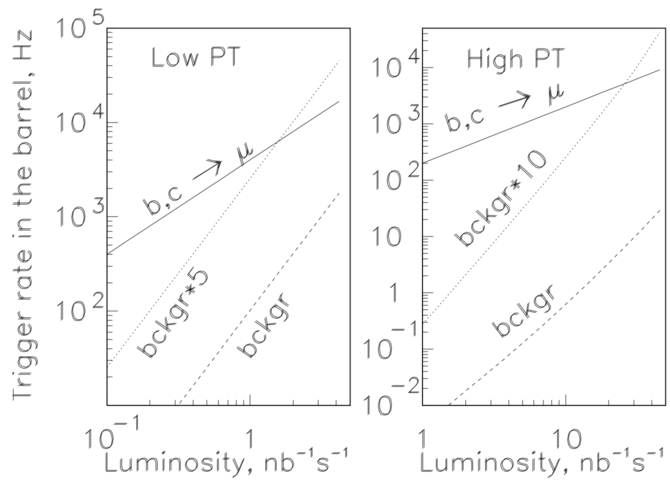

Figure 2: Low and High-p_T trigger rate in $|\ \eta\ | < 1.05$ as a function of the luminosity

2.1. Trigger segmentation, ROI's

The trigger detectors in the barrel are segmented in 24 ϕ sectors: 16 between the coils (large sectors) and 8 close to the coils (small sectors). Along the z axis the segmentation is projective to the interaction vertex. While the segmentation of the detector itself comes mainly from the geometry of the experiment.

The p_T threshold of the first level trigger (L1) will be refined at second level (L2), by using the high precision chambers' information. The L1 will provide Regions Of Interest (ROI), where the L2 processor will search for muon tracks in small sectors of the spectrometer.

The L2 algorithm is initiated by the L1 strip information that has an average occupancy much smaller than the precision drift chamber. A good compromise between layout considerations and L2 needs is a segmentation $\Delta\eta \times \Delta\phi \sim 0.13 \times 0.10$. In this case the barrel will be equipped with 2304 matrices of 32×64 strips.

3. The Muon trigger processor

To be able to uniquely identify tracks belonging to a bunch crossing, it is not only necessary to have a fast detector, but the trigger electronics itself must have a time resolution comparable to the detector. Moreover the trigger has to be multithreshold, allowing multimuon events to be selected with thresholds lower than the single muon ones. Six thresholds will be programmable in the range $5 - 35\ GeV/c$.

All the previous needs are best met by developing an Application Specific Integrated Circuit (ASIC), which will be mounted locally on the detector, close to the frontend electronics. The gathering of data for the local logic will be done by 48 Sector Logic processors (SLP), each reading 24 $r - z$ and 24 $r - \phi$ matrix outputs, covering 24 ROIs.

The main function of the SLP is to concentrate L1 data, cluster together hits from the same track, associate tracks in the two projections and eliminate double counting of tracks giving hits in two or more ROIs. The SLP output will be concentrated to the Global μ trigger through 96 links running at 800 $Mbit/s$. The Global μ Trigger (GMT) will generate total multiplicity for each of the 6 thresholds and send this information to the L1 Main processor at the 40 MHz bunch crossing frequency. In the sector and global μ logic more detailed information will be stored for the ROI builder and sent via the L2 readout links to the L2 buffers.

The total expected data rate does not exceed 10 $Mbyte/s$, while the detector data will be around 70 $Mbyte/s$. The total L1 latency is less than 1.5 μs.

3.1. Synchronization

Due to the large area of the detector, timing is a critical issue; propagation time along different regions of the detector, as well particles time of flight can be longer than 25 ns. The ATLAS Timing Control and Distribution System [11], will be used as the starting point by providing a reference $f_B = 40\ MHz$ clock and a programmable bunch crossing number. Finer sub-period delays will be implemented using programmable depth micropipelines, for unique assignment of a track to a bunch crossing. A time interpolator running at $4f_B$ or $8f_B$ frequency will be needed to monitor these delays.

3.2. The coincidence matrix

We have realized a 0.5 μm CMOS $34K$ gate array [12] for the front-end part of the trigger system. The demonstrator circuit contains two

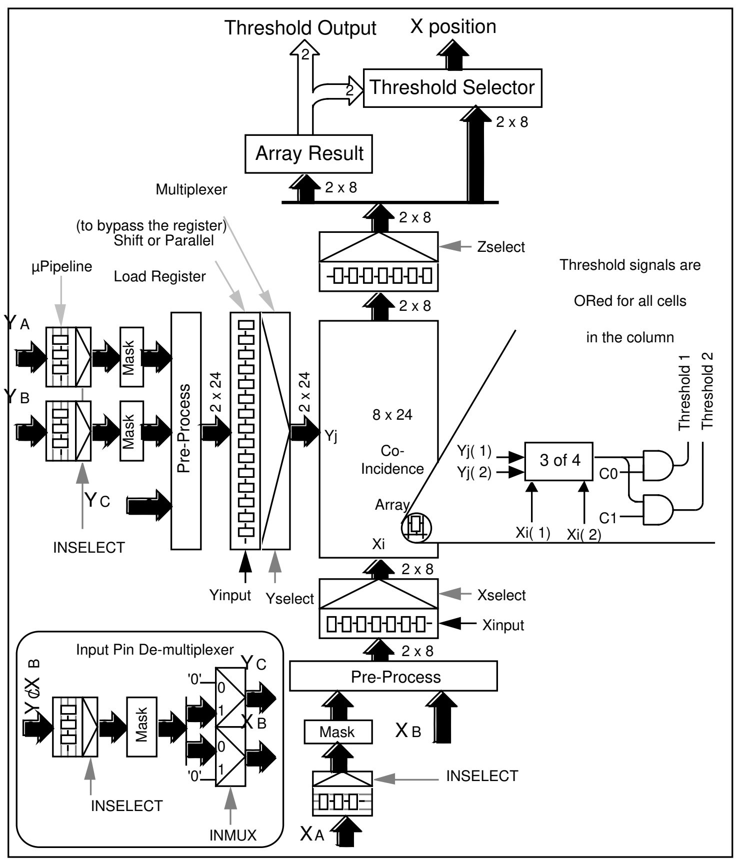

Figure 3: Block diagram of the coincidence matrix ASIC

8×24 coincidence matrices. The $low - p_T$ and $high - p_T$ algorithms can be implemented programming the same circuit for the two modes of operation.

The detector signals, after discrimination, are fed into a micropipeline running at a frequency multiple of f_B. This is done to compensate for different propagation times from different detector planes. The 3/4 or 2/3 majority algorithm is done in two steps; one part is common to all the columns or rows of the matrix (Pre-Process blocks), while the other has to be done cell by cell. The (most significant) hit pattern of the muon track(s) is fed into an output register, together with the threshold value the track(s) has (have) passed. The logic is distributed over an internal pipeline of maximum 4 steps lenght.

The circuit can operate in fully pipelined mode, fully combinatorial, or any combination of the two. Additional test facilities and the possibility of masking noisy channels or missing planes have been realized within the gate array cell quota. All internal registers are accessed by a dedicated serial input and output lines. The die operates at 3.3 V and is mounted on a 120 pin QFP package.

Laboratory tests have proved that the maximum skew between different inputs to different outputs is below 1.8 ns, maximum operating frequency is above 100 MHz, total processing time in fully combinatorial mode is $\simeq 7$ ns, the same for the two trigger algorithms.

A dedicated VME board has been designed for testing the ASIC in a test beam. The board is a 6U VME board with 80 differential ECL inputs (four detector planes) and 8 differential ECL outputs (most significant trigger pattern). Two NIM inputs are used for fast clear and for the external clock. Two NIM outputs provide the threshold outputs. The interface between the VMEbus and the ASIC internal registers is realized with a *Field Programmable Gate Array* (FPGA) Xilinx 3042 which converts parallel longwords into variable lenght serial words and vice versa. The ASIC run mode and clock settings can be changed via this FPGA.

3.3. Beam tests

These circuits have been tested in a test beam at CERN with RPCs illuminated by 180 GeV/c muons. The trigger hodoscope used seven chambers with orthogonal strips of 3 cm pitch to identify muons in two projections, and was arranged in two doublets and a triplet, respectively 40 cm and 200 cm apart. The test trigger system is shown in figure 4. The RPC were operated in avalanche mode [13]. The gas was a mixture of Tetrafluor-ethane (0.95) and Isobuthane(0.05) [14]. The RPC signals were amplified with a two-stage bipolar fast amplifier [15] and

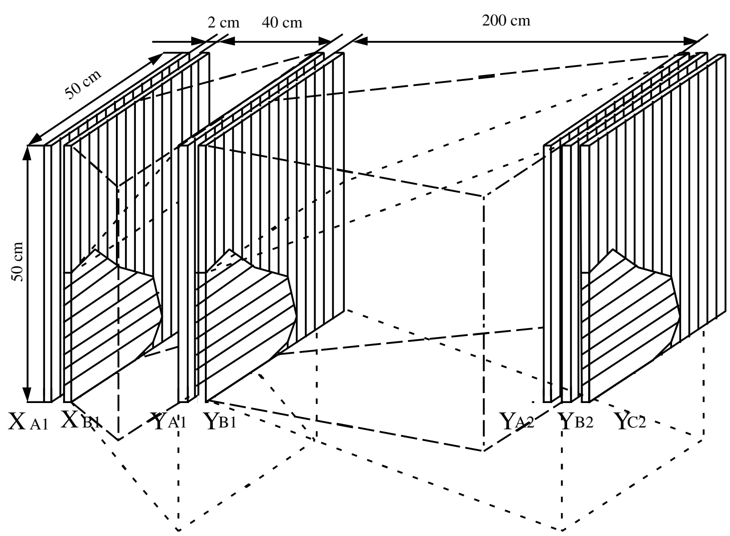

Figure 4: The RPC trigger tower. The dotted lines are regions covered by one matrix

discriminated with standard circuits.

In total eight trigger boards were needed to trigger on both projections and 224 (chambers) + 80 (trigger) channels were digitized by standard 1 ns LSB multihit TDCs. In figure 5 the Time of flight between the two doublets and between the first doublet and the triplets are shown; a $\sigma \simeq 3$ ns is measured. In figure 6 the time response of the low and high p_t coincidence matrices, is shown for both projections. A processing time of the $high - p_t$ algorithm of $\simeq 13$ ns is measured time of flight and interconnecting cables. The integrated detector/electronics time resolution is $\simeq 2$ ns.

4. Conclusions

The ATLAS level 1 muon trigger logic is designed to make unique bunch crossing ID and provide sharp thresholds over a wide range of transverse momenta. The local trigger logic has been succesfully designed and tested, based on a 0.5 μm CMOS circuit ($Fujitsu\ CG51$). The ASIC performed as expected.

This technology is already mature to fulfill our needs of low prop-

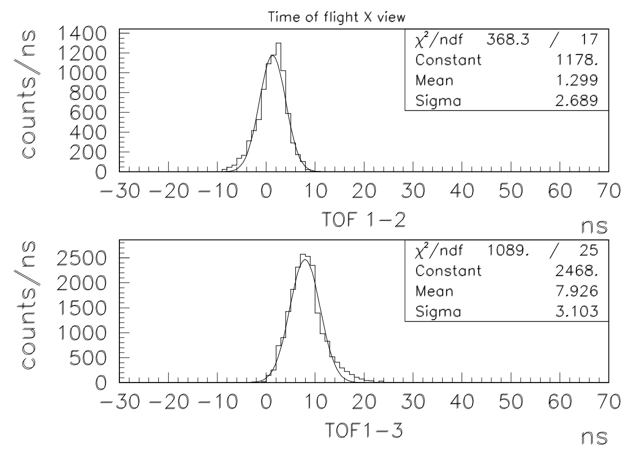

Figure 5: time of flight between the two doublets(top) and the first doublet and the triplet(bottom)

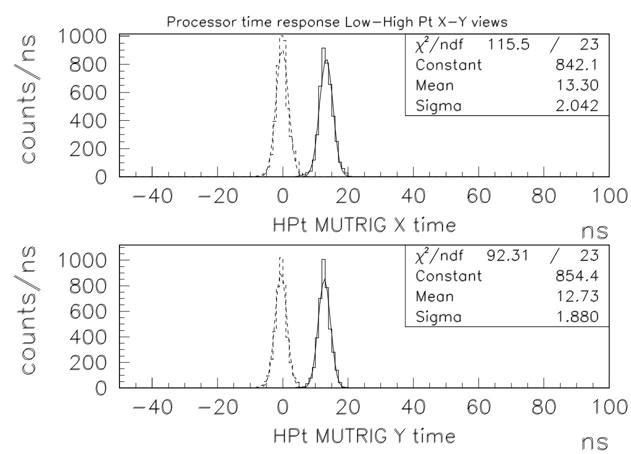

Figure 6: Trigger system time response on the two projections. The dotted line distribution is the $low - p_T$ processor response while the full line distribution is the $high - p_T$ processors response

agation time and integration. The final implementation will simply be scaled to a 32×48 coincidence (100k gates required). Faster IO will be used to provide the necessary $160 - 320$ MHz needed in the experiment. The current technology already uses differential PECL to drive signals at frequencies in excess of 350 MHz.

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14. see V. Makeev contribution to this conference.

15. see R. Cardarelli contribution to this conference.