CERN/LHCC 96–4
LERB Status Report / RD27
20 December 1995

FIRST-LEVEL TRIGGER SYSTEMS FOR LHC EXPERIMENTS

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1. Introduction

The RD27 project [1] was approved in June 1992 [2] to perform a broad-based study of first-level trigger systems. The progress of the project was reported in Summer 1993 [3] and in January 1995 [4]. Continuation of the project for a further year was approved [5] with the following milestones:

- Beam tests of a second-generation muon-trigger processor incorporating a coincidence-matrix ASIC.
- Beam tests of bunch-crossing identification logic for the calorimeter based on FPGAs, using a new FADC system.
- Evaluation of key components of the central trigger processor in gate arrays.
- Development of demonstrators for key components of calorimeter trigger processors including evaluation of:
  - fast optical links and integrated optics;
  - fast electrical data transmission between boards and crates;
  - fast high-density processing ASICs.
- Submission of a bit-serial demonstrator ASIC to a manufacturer.

Members of RD27 are very active in ATLAS [6] and CMS [7]. In particular, design work for the ATLAS calorimeter, muon and central trigger processors, and for the CMS calorimeter trigger processor, is being performed by RD27 groups. Members of RD27 (N. Ellis and W. Smith) are the trigger coordinators for the two proposed LHC experiments.

Given that the approval process for ATLAS and CMS is now well advanced, much of the work that was started within RD27 is now organised and funded by the LHC experiments. However, there are a number of areas where we consider that continued collaboration for one more year within RD27 will be valuable:

- High-speed, synchronous data links for transmitting data to trigger processors.
- High-speed custom backplanes for inter-module communication within trigger processors.
- Assessment of FPGAs as components for trigger processors, especially in the central trigger processor where the number of processing units required does not justify a custom circuit development.
- Evaluation of alternative ASIC technologies and designs.

All of the above are continuations of ongoing work. The results obtained will allow both ATLAS and CMS to benefit from a broader assessment of these items than would otherwise be possible. The use of resources will be optimised because R&D will not be duplicated in the two experiments, and some sharing of specialist test facilities may be possible. It is possible that, as a result of this collaboration, the two experiments will adopt common solutions within their trigger systems.

In this document we report on the work that has been performed and propose a programme of R&D for the next 12 months. It is our intention to complete the programme of work of RD27 in the coming year, after which we will submit a final status report documenting our work. In the longer term, we plan to continue to hold regular meetings between first-level trigger experts from ATLAS and CMS to promote the exchange of ideas and adoption of common solutions where appropriate. In the following, we discuss in turn the muon, calorimeter and central trigger processors, and suggest milestones for the coming year. In each section, we indicate whether any continuation of the work is part of the proposed RD27 R&D programme, or whether it will be pursued within the ATLAS and CMS trigger projects.

3. Muon Trigger

The programme of work on the muon trigger processor, proposed in our last status report [4], was successfully carried out. A demonstrator system, incorporating a coincidence-matrix ASIC, was tested at the H8 test beam using signals from RPC detectors. More details of this work were reported [8] in the recent LERB workshop in Lisbon.

Programmable coincidence matrix ASIC

The coincidence-matrix ASIC [9] was developed by Rome with help from the RAL electronics group. It consists of 8×24 elements, each of which can be programmed for two independent coincidence conditions corresponding to different p_T thresholds. The ASIC can operate in two modes, corresponding to the low and high-p_T muon trigger conditions in ATLAS (see Figs. 1 and 2). In the first mode it requires a three-out-of-four multiplicity in a pair of chamber double layers; in the second mode it requires a two-out-of-three multiplicity in a chamber triplet, in coincidence with the output from the low-p_T logic.

The ASIC can be operated in fully-combinatorial mode which offers excellent time resolution for the trigger condition, with possible application for rejecting background on the basis of the time-of-flight between muon chamber layers. It can also be operated in pipelined mode, in which case the input signals can be delayed by a programmable number of clock cycles to compensate for different propagation delays upstream of the trigger logic; the delays for the X and Y inputs are programmable independently.

The ASIC was implemented in a 0.5 µm CMOS gate array from Fujitsu (34k gates). The measured maximum skew is 1.8 ns, and the device can operate at clock speeds up to 130 MHz giving good time resolution even when operated in pipelined mode. A block diagram of the ASIC is shown in Fig. 3.

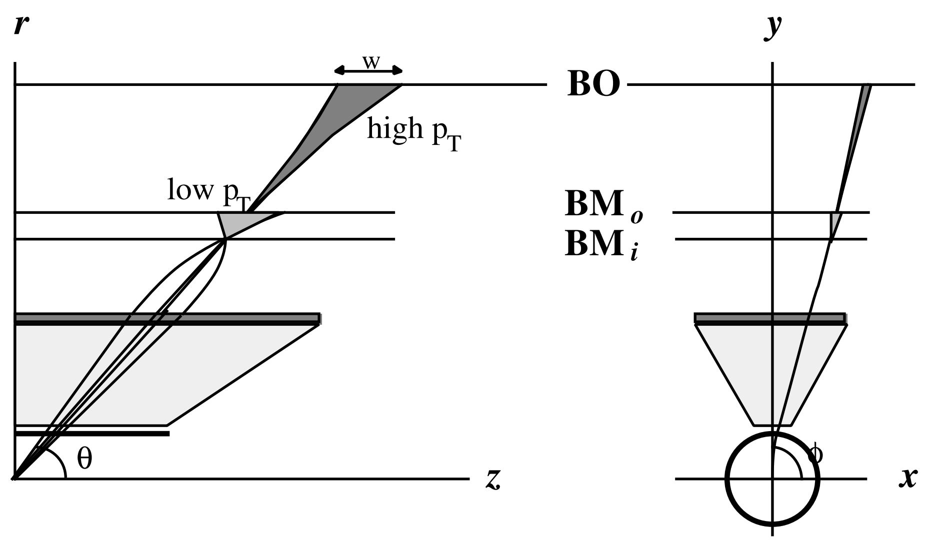

Figure 1: Conceptual design of the first-level muon trigger for ATLAS.

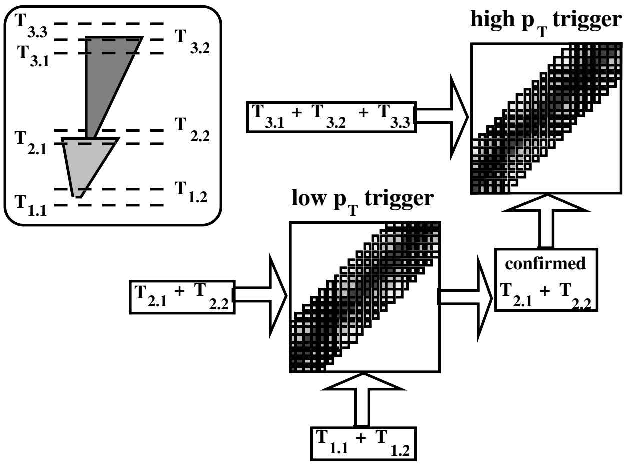

Figure 2. Muon trigger local logic for one projection. The symbols $T_{i.j}$ refer to trigger chamber layers located at different points in the spectrometer. The inputs to the two axes of the coincidence-matrix circuits are the patterns of hits in the different chamber layers. The matrix is programmed to identify combinations of hits that correspond to valid tracks for the different p_T thresholds.

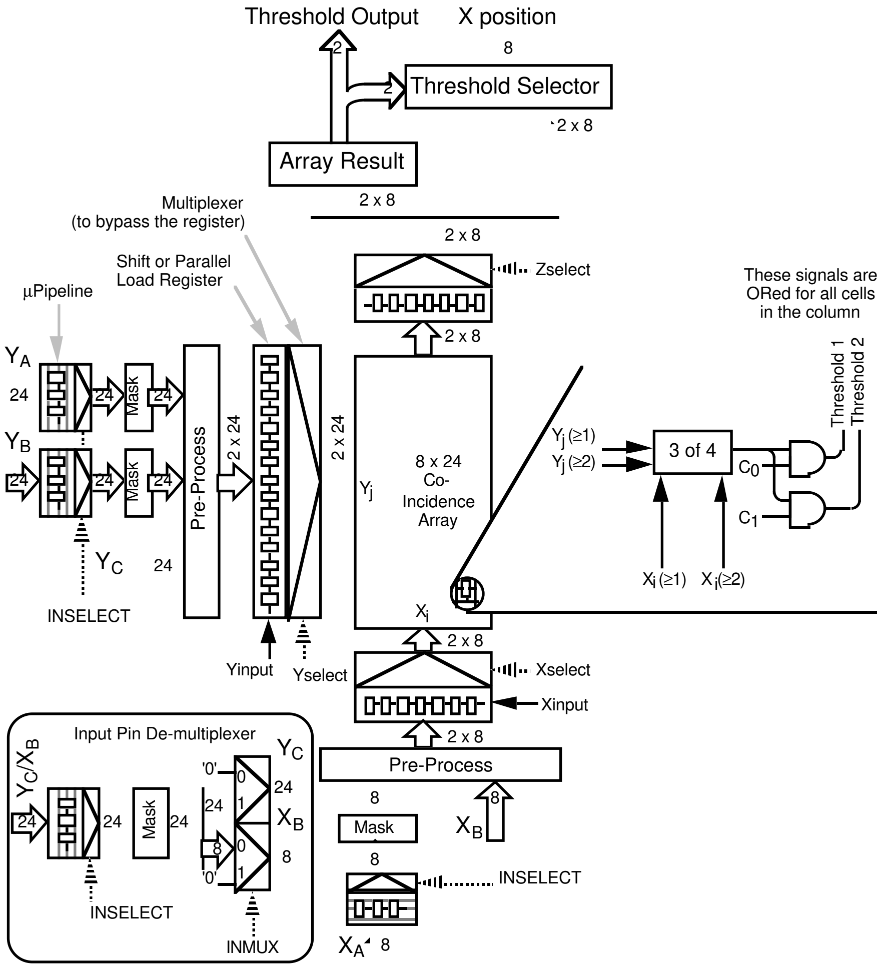

Figure 3: Block diagram of muon-trigger demonstrator ASIC.

Second-generation muon-trigger processor demonstrator

A muon-trigger processor demonstrator was implemented by the Rome group based on the coincidence-matrix ASICs. VME modules were manufactured, each supporting one ASIC.

Inputs to the ASICs arrive via front-panel connectors using ECL differential signals. The output signals leave the modules also via front-panel connectors using ECL differential signals. This modular system allows the ASICs to be configured in different ways to implement the so-called low-p_T and high-p_T trigger logic. Inputs to the system were discriminated signals from the muon-trigger chambers.

Beam tests at H8 test beam

A total of eight of the demonstrator modules described above were used to implement a trigger at the H8 test beam, using signals from RPC chambers. The "trigger tower" measured about 50 cm by 50 cm, with seven layers per projection in a similar arrangement to the one planned for ATLAS. The system worked as expected, with excellent time stability (~2 ns) and low latency (about 30 ns in total, 15 ns for the low-p_T trigger condition and a further 15 ns for the high-p_T one), as illustrated in Fig. 4.

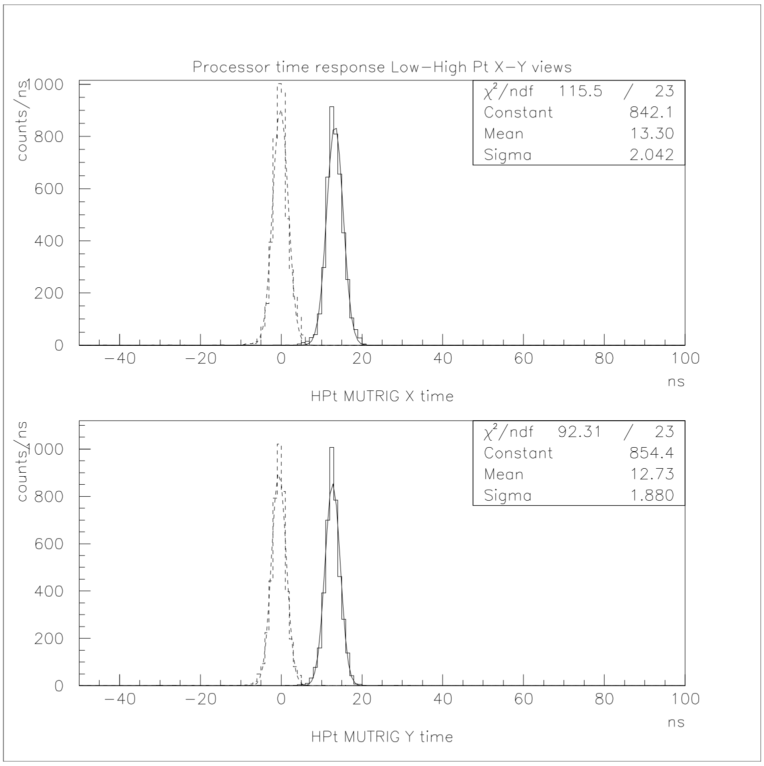

Figure 4: Real-time performance of the muon-trigger demonstrator prototype. The upper plot shows the time distribution of the output of the low-p_T (dashed curve) and high-p_T (solid curve) logic, for the x-coordinate RPC strips. The lower plot shows the same distributions for the orthogonal y projection.

During 1996 it is planned to use the same system to make tests with full-area trigger chambers, as part of the ATLAS first-level trigger project. This work will address the problems of synchronisation over large areas, making use of standard (RD12) TTC components when available.

3. Calorimeter Trigger

A large amount of work has been performed in the last year relating to the calorimeter triggers for ATLAS and CMS. Some of this work was reported at the recent LERB workshop in Lisbon [10–14]. As an aside, it is interesting to note that a substantial fraction of the work is being carried out following a formalised quality system based on ISO9001 [15].

New FADC system

An ADC system has been constructed by the Heidelberg group for use in tests of calorimeter trigger processors. Each FADC board is a standard VME module containing four channels with 8-bit resolution. An external clock input allows sampling rates of more than 80 MHz. The key feature is the front-panel output of digitised data in real time to the subsequent trigger logic. So far 12 ADC modules have been built, and 11 more will be constructed.

In addition to the ADC function, each channel is equipped with a scrolling memory which records the most recent 256 samples. This memory can be read out when digitisation is stopped by a gate signal. The memory is read/write accessible from VME, and the modules can be used in "playback" mode in order to test the subsequent trigger logic.

A detailed description of the FADC module can be found in Ref. [16]. An example of a recorded pulse from a prototype liquid-argon calorimeter is shown in the upper plot of Fig. 5.

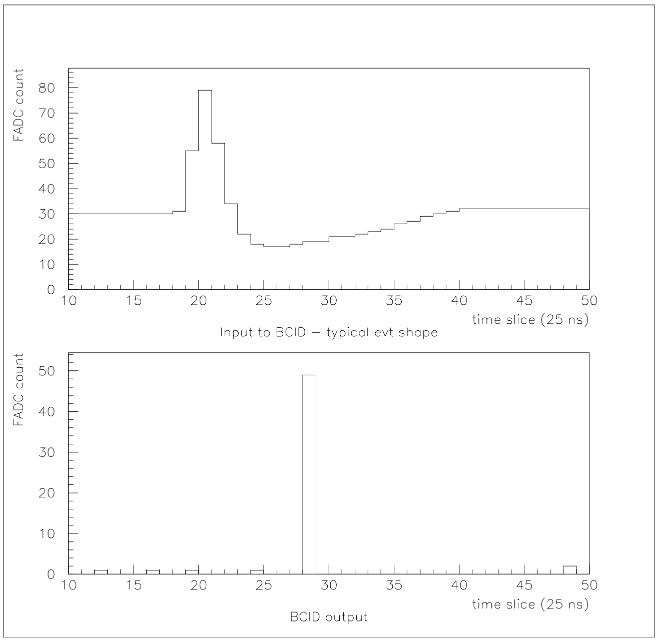

Figure 5: Example of calorimeter pulse recorded with the ADC system.
The upper plot shows the pulse as recorded by the FADC system.
The lower plot shows the output of the real-time bunch-crossing-identification processing.

The new FADC system has been used to test prototype trigger systems, sending the data over a differential-ECL crate-to-crate link. This work will continue within the ATLAS first-level trigger project.

Bunch-crossing identification studies at the test beam

Given that the response time of calorimeters at LHC will be longer than the 25 ns interval between bunch crossings, it is necessary to perform bunch-crossing identification (BCID) processing. Digital signal-processing algorithms are being studied in RD27 that convert a calorimeter pulse that spans several ADC samplings to a signal that appears only in a single time bin, corresponding to the bunch crossing that gave rise to the energy deposition. The algorithms that have been implemented consist of a finite impulse response (FIR) filter, followed by a peak finder, as illustrated in Fig. 6.

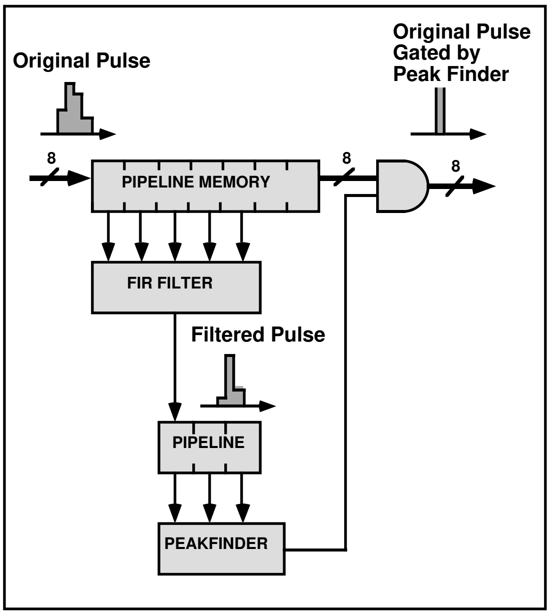

Figure 6: Block diagram of BCID logic.

In our last status report, we reported on initial studies with a single-channel demonstrator prototype based on discrete logic. During the last year, the UK groups have implemented a multi-channel demonstrator prototype based on FPGAs. Each 9U module handles 12 channels of 8-bit input data from the ADC system described above; each of three FPGAs handles BCID processing for four channels. In addition to the work with FPGAs, a first ASIC implementation of a four-channel BCID processor has been implemented by the Heidelberg group. The ASIC was designed so that it could replace the FPGA processing elements in the demonstrator system by using an adapter board.

Bunch-crossing identification has been successfully performed on calorimeter signals in real time using the FPGA system programmed with various algorithms, and using the ASICs. The test-beam setup is illustrated in Fig. 7. An example of the output from the BCID demonstrator is shown in the lower plot of Fig. 5. Good efficiency is obtained for energies above about 2 GeV, which is adequate for triggering at LHC. Work is continuing to optimise algorithms for very small and very large pulses. More details on the BCID studies can be found in Refs. [11, 14]. This work will be continued as part of the ATLAS first-level trigger project.

Studies of fast input data links

A major challenge for the calorimeter trigger processors of ATLAS and CMS is the data rate into these systems. With about 8000 8-bit words of input data per 25 ns period, the total data rate is 2560 Gb/s to which must be added the overheads associated with framing, error detecting codes, etc. Special requirements for the first-level trigger are synchronous links with fixed low latency. In the Technical Proposal designs, both experiments assume ~ 1 Gb/s links each carrying data for two trigger cells; both experiments consider the possibility of using the HP G-link chipset (HDMP–1012/1014).

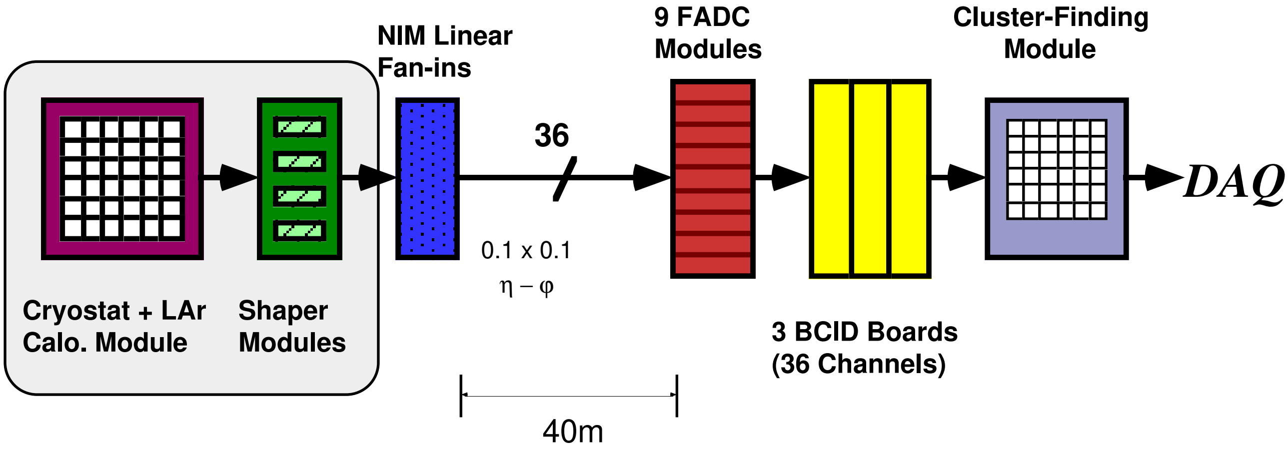

Figure 7: BCID evaluation system used in 1995 test-beam running

A number of developments are in progress within RD27 related to the fast data links. We are looking at the possible use of serial electrical links as an alternative to optical ones in case the digitisation system is placed in close proximity to the trigger processor.

An evaluation is currently being made of optical links using the HP G-link chipset and Finisar optical transmitter/receiver modules (FTM–8510 and FRM–8510). Demonstrator modules designed at RAL for the BaBar experiment were modified to operate in simplex mode for this work, and preliminary tests have been made running the links at 75 MHz with 20-bit frames and at 80 MHz using 16-bit frames. Initial results are encouraging and of considerable significance as they open the possibility of transmitting data from four, instead of two, trigger cells per link, with important implications for the cost of trigger systems.

An alternative to using the HP G-link chipset would be a custom solution making use of the availability of a common 40 MHz clock at the transmit and receive ends of the data links. This approach is addressed by the bit-serial test ASIC development discussed below.

Commercial optical/electrical components and chipsets tend to be physically quite large. Our application is unusual in the requirement to bring tens or even hundreds of optical fibres onto individual circuit boards. This has led us to consider novel solutions such as integrated optics and multi-chip modules (MCMs) containing unpackaged components (e.g. unpackaged G-link circuits).

During 1996, initial studies of the input data links will be made using a modular demonstrator system with discrete optical/electrical conversion and serial/parallel conversion components mounted on a daughter-board. However, provision has been made to include an MCM containing optical/electrical conversion and serial/parallel conversion at a later stage. A decision to proceed with an integrated-optics MCM awaits a choice within ATLAS on the location of the trigger digitisation system, in view of the significant non-recurring engineering cost and funding limitations.

While we have not yet manufactured an integrated-optics MCM, detailed design studies have been made for a four-channel circuit, including extensive consultation with industry. The result of these evaluations is that such circuits are feasible, and several companies have offered to build them. We also have recently contracted GEC-Marconi to perform a technology evaluation for a higher-density integrated-optics system.

In view of the common interest of the LHC experiments, it is proposed to continue this work during 1996 within the RD27 project.

Studies of high-speed backplanes

Studies are under way for high-speed custom backplanes for inter-module communication. The Wisconsin group and UK groups have designed 160 MHz backplanes based on differential-ECL and on BTL signal levels, respectively. The BTL backplane has recently been manufactured, and it will be evaluated during 1996. The ECL backplane will be built and evaluated during 1996. The Stockholm group is investigating the possibility of a 320 MHz backplane based on LVDS differential signals. All of the above backplanes are for point-to-point connections and use impedance-matched lines for the high-speed signal transmission. In the processor systems, they would be accompanied by conventional backplane buses for test, control, monitoring and readout. All the above are considered in the context of conventional 9U crate mechanics.

In view of the generic nature of the studies on high-speed custom backplanes, we propose to retain this work in the RD27 programme for 1996.

Development of fast, high-density processing ASICs

A number of ASIC developments related to calorimeter trigger processors have been made during the last year.

High-speed adder ASIC

A very high-speed adder ASIC, designed by the Wisconsin group and illustrated in Fig. 8, has been manufactured using a 0.6 µm GaAs process from Vitesse. This ASIC has eight operands of 13 bits, consisting of 10 bits of value, one bit of sign, one bit of input-value overflow and one bit of arithmetic overflow. The ASICs can be connected together to form an adder tree, propagating the information on the two kinds of overflow. A design requirement was that the ASIC should work at 160 MHz, allowing four sets of additions to be performed in every 25 ns period. In fact it has been tested to 200 MHz (limited by the available test facilities) and simulation shows that it should function correctly at above 300 MHz. The ASICs may be tested at higher speeds using specialist facilities in Heidelberg. The ASICs (and the design) are available for use by both ATLAS and CMS. More details on this ASIC can be found in Refs. [4, 10].

Dual-function multiplexer/demultiplexer ASIC

A dual-function multiplexing/demultiplexing ASIC, illustrated in Fig. 9, has been designed by the UK groups and manufactured. Used in its first mode, it multiplexes 16 bits of data at 40 MHz into four bits of data at 160 MHz. In its second mode it performs the inverse operation. These two functions were combined in a single device for reasons of economy in the demonstrator system. The purpose is to reduce by a factor of four the number of physical connections between components in the trigger system, by running at a speed four times higher than the bunch-crossing frequency. This ASIC was manufactured by ES2 in a 0.7 µm CMOS process. Seventy packaged chips have been delivered and all have been successfully tested at RAL at 160 MHz; a subset of the chips is being tested at higher speeds in Heidelberg.

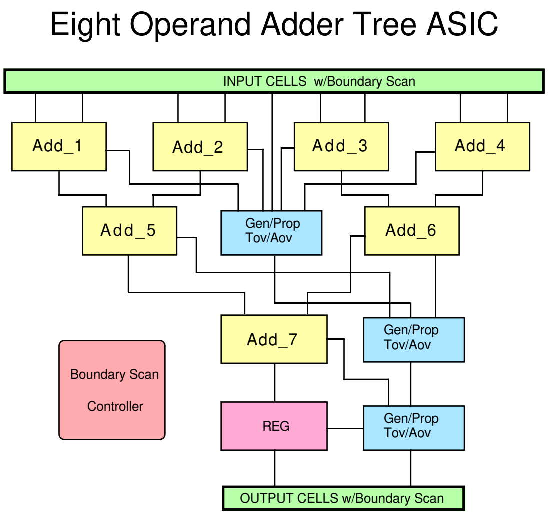

Figure 8: Block diagram of high-speed adder ASIC.

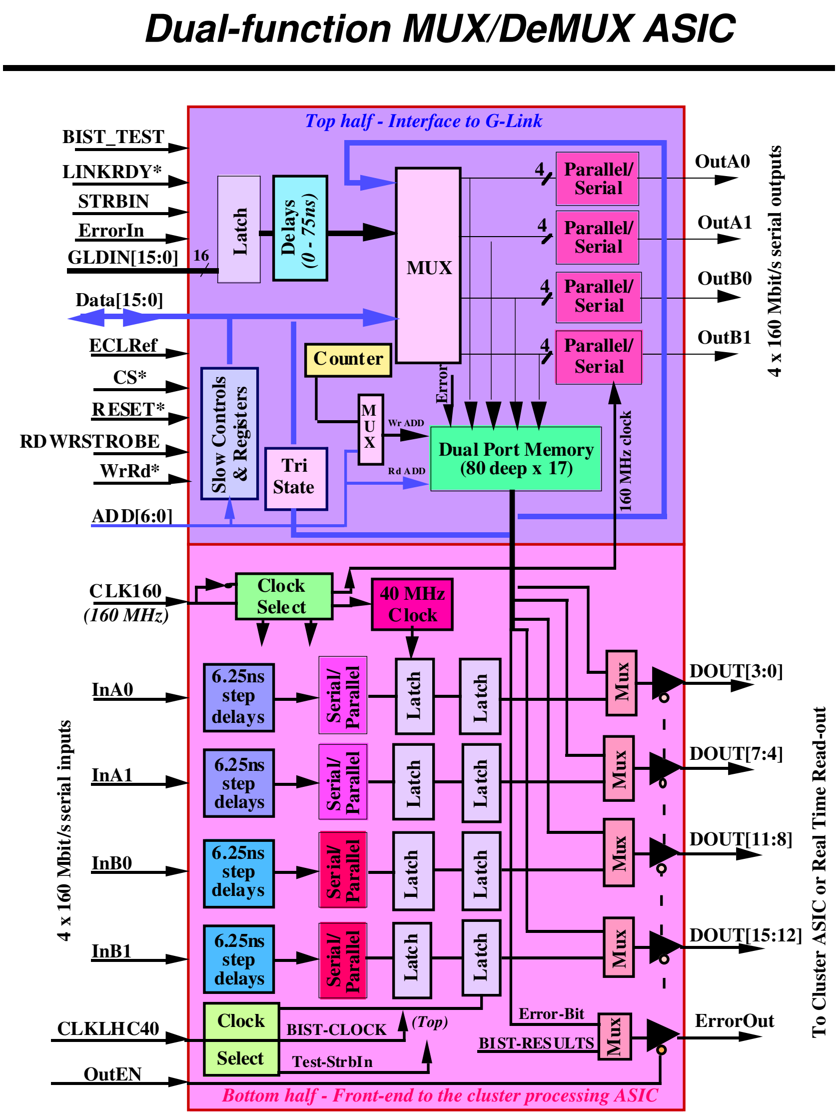

Figure 9: Dual-function ASIC block diagram.

Bit-serial test ASIC

A test ASIC for the 800 MHz input part of the bit-serial processor development [13] has been designed by the Stockholm and Linköping groups, and submitted for manufacture. This will receive 16 serial inputs at 800 MHz, and perform serial-to-parallel conversion. As shown in Fig. 10, the input data are received differentially. The logic delays the signal with a suitable programmable delay of up to one bit in duration; this analog delay will be chosen such that the subsequent sampling unit will sense the signal at an optimal position for proper bit alignment. The sampling is controlled by five phase-delayed local 160 MHz clocks, generated from the 40 MHz master clock. The ASIC is being manufactured in a 0.6 μm BiCMOS process by Ericsson, and delivery is scheduled for February 1996. Testing of this ASIC will be performed in Stockholm and in Heidelberg.

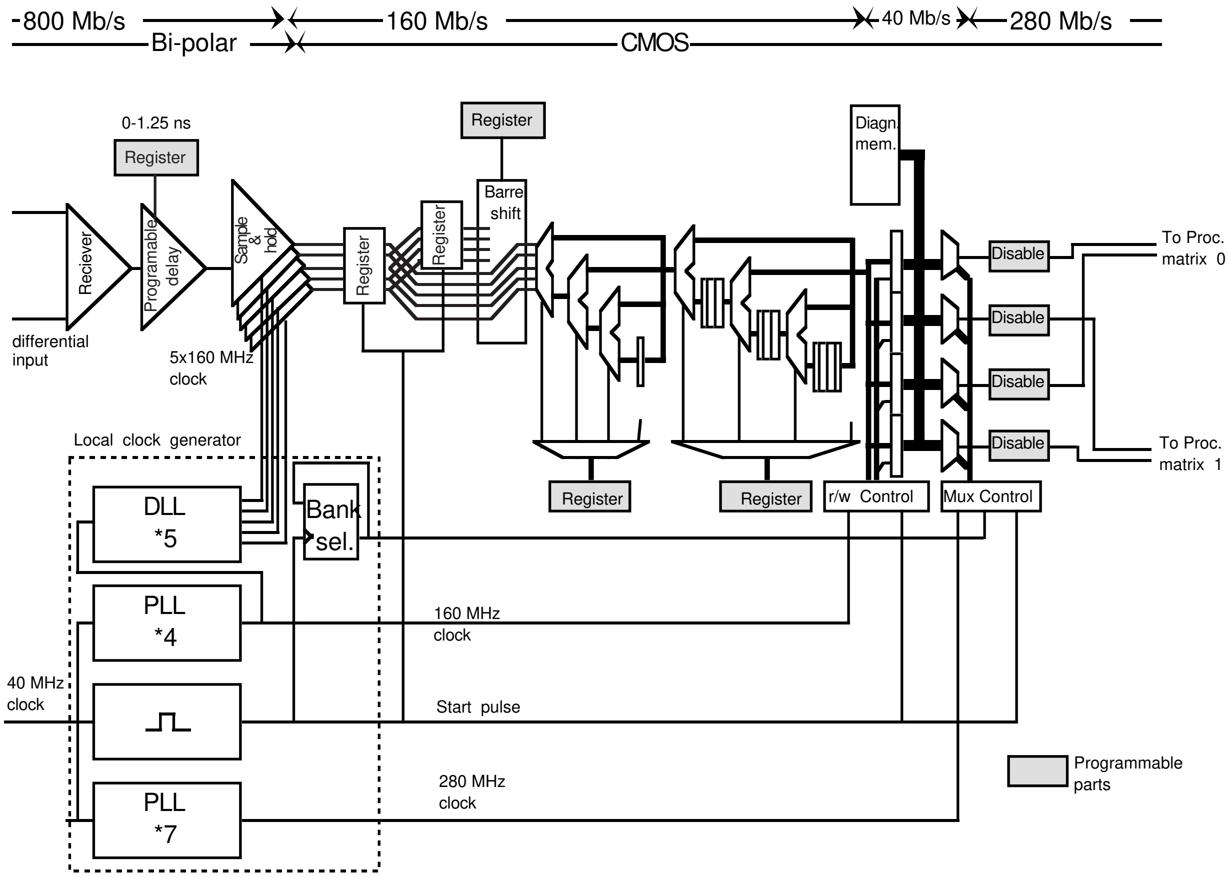

Figure 10: Block diagram of the input stage for one channel in the bit-serial development.

Bunch-crossing identification ASIC

The BCID ASIC discussed above and in Ref. [14] should also be mentioned here. This was designed in Heidelberg and manufactured in a 1 μm process by ES2. It was tested in the laboratory and then successfully integrated in the demonstrator system at the test beam. It is planned to develop and manufacture a second-generation BCID ASIC that will include additional functions: look-up tables for calibrating the input data, pipelined readout with a derandomising buffer for deadtime-less operation, and a test facility consisting of “playback memory”.

The ASICs described here, developed and evaluated in the context of the RD27 collaboration, will be included in demonstrator prototype systems for the first-level triggers of ATLAS and CMS.