4. Central Trigger Processor

Design by the CERN group of a central trigger processor (CTP) demonstrator is well advanced. This demonstrator will contain all the essential elements of a final system, and will work at full speed with the required low latency (≤ 125 ns). However, it will not have as many inputs or allow as many combinations as would be needed for a final system.

We had originally envisaged using custom gate arrays for the CTP. However, it was found that sufficiently large and fast FPGAs are now available to construct a compact system that can operate within the required low latency. A study has been performed of the feasibility of implementing the key components of the CTP in FPGAs. Following an initial evaluation [17], almost all of the system has been designed.

As for other parts of the trigger processor system, we are planning to install the CTP demonstrator at the H8 test beam where it will be connected to the calorimeter trigger processor. Such tests are useful to check the completeness and robustness of the system.

Components of the CTP

A block diagram of the CTP demonstrator is shown in Fig. 11. Signals from subtrigger processors such as the calorimeter trigger processor arrive in groups of four, each group accompanied by a clock signal that indicates when the signals are stable. The first block in the CTP logic, labelled VLPL, is responsible for alignment of the different groups of signals in time. The synchronisation step latches the input on the leading or trailing edge of the local clock, the choice being made so that the input data are sampled when they are stable. The following alignment step allows one to introduce a delay of an integer number of bunch crossings. Alignment of the 32 input signals will be performed in a single FPGA circuit, reconfigurable in situ to adjust the delays.

The next block in the CTP, labelled LUT, performs the trigger algorithm which allows combinations of the inputs to be required in coincidence, veto or “don’t care”. It is implemented using a combination of SRAM and discrete logic. Up to 32 combinations of the 32 inputs can be defined, corresponding to 32 independent trigger conditions, the OR of which is the event trigger. We have also investigated a design for this logic using FPGAs; while this would also be feasible, we have chosen the SRAM solution for the demonstrator because of its flexibility, ease of programming and low latency.

Following the LUT, the next block contains mask and veto logic. This allows individual triggers to be masked, for example to introduce deadtime preferentially for low priority triggers, or for a global veto to applied. The latter can be used to impose deadtime globally; for example to introduce a minimum interval between consecutive first-level triggers.

Next in the data flow is the prescaler block that allows the 32 triggers to be prescaled by independently programmable factors. For the demonstrator, 12-bit prescalers will be provided, but larger factors could be implemented for a final system. Each FPGA will include 16 prescalers.

The final stages in the CTP are the OR over the 32 individual trigger conditions, followed by logic that determines when deadtime should be introduced as required by constraints in front-end electronic systems.

A number of essential additional facilities are included in the design. TDCs are provided that measure the phase of the clock signals accompanying the input data relative to the local

clock; these are needed to assist in setting up the timing of the system. A test memory is provided to generate a long pattern of input data, up to 25 ms at the nominal speed. A facility to generate pseudo-random bit sequences is also included.

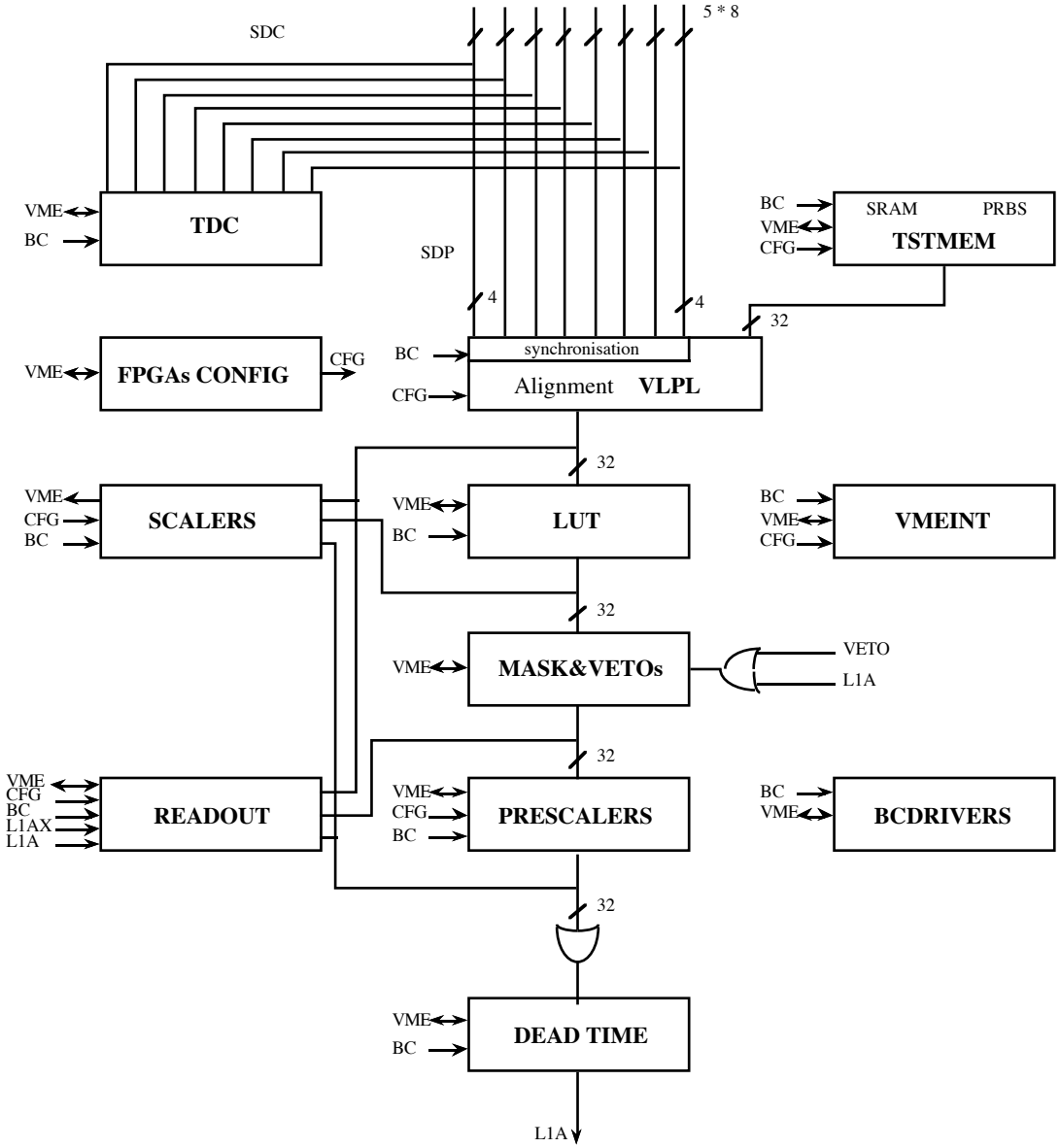

Figure 11: Block diagram of the CTP demonstrator.

Scalers monitor the rates at various points in the system — each of the 32 inputs, each of the 32 trigger combinations and each of the 32 combinations after prescaling. The scalers are implemented using FPGAs. Each circuit contains 32 12-bit scalers with associated read-out registers. This allows scaling for a complete cycle of the LHC machine (88 μs), with readout of the read-out register between cycles.

For triggered events, results will be read out from various parts of the system — the pattern of inputs, and the pattern of outputs before and after prescaling. This requires pipeline memories and derandomising buffers as for detector readout systems. The system will allow a time frame to be read out with a width programmable over the range 3–5 bunch crossings; this will be helpful when setting up the system. For the demonstrator system, the "derandomizer" will be implemented as a FIFO. For beam tests, the FIFO will be read out between bursts.

The status of the system is that all of the FPGA parts have been designed and simulated. The demonstrator will be implemented as a 9U VME module which will be tested in the laboratory and at the test beam during 1996. The results of these evaluations and the designs for the FPGAs will be available for use by the LHC experiments.

The CTP development is of general interest to the LHC experiments, all of which will need components such as prescalers, scalers, etc. In contrast to the calorimeter and muon trigger processors, the CTP design does not depend strongly on the particuliarities of the detectors. We therefore propose to continue the work on the CTP demonstrator within RD27 for a final year.

5. Suggested milestones

We propose the following milestones for the final year of the project, focusing on items that are part of our ongoing programme and are of common interest across the LHC experiments:

- Tests of very high-speed (≥ 800 Mbit/s) synchronous serial data links for transmitting data to trigger processors.
- Tests of high-speed (≥ 160 Mbit/s) custom backplanes, based on BTL and differential-ECL signals, for communication between trigger-processor modules.
- Provision of demonstrator systems for central trigger processors based on FPGAs.

6. Request to CERN

We request funding from CERN at the level of 65 kCHF in 1995; there is no overlap of this request with the requests made by the ATLAS and CMS collaborations. We also request continued electronic-engineering support from ECP division at the same level as in 1995; this is required for the work on the central trigger processor demonstrator.

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