RD27

FIRST-LEVEL TRIGGER SYSTEMS FOR LHC EXPERIMENTS

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CERN

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INFN and Universita La Sapienza, Rome

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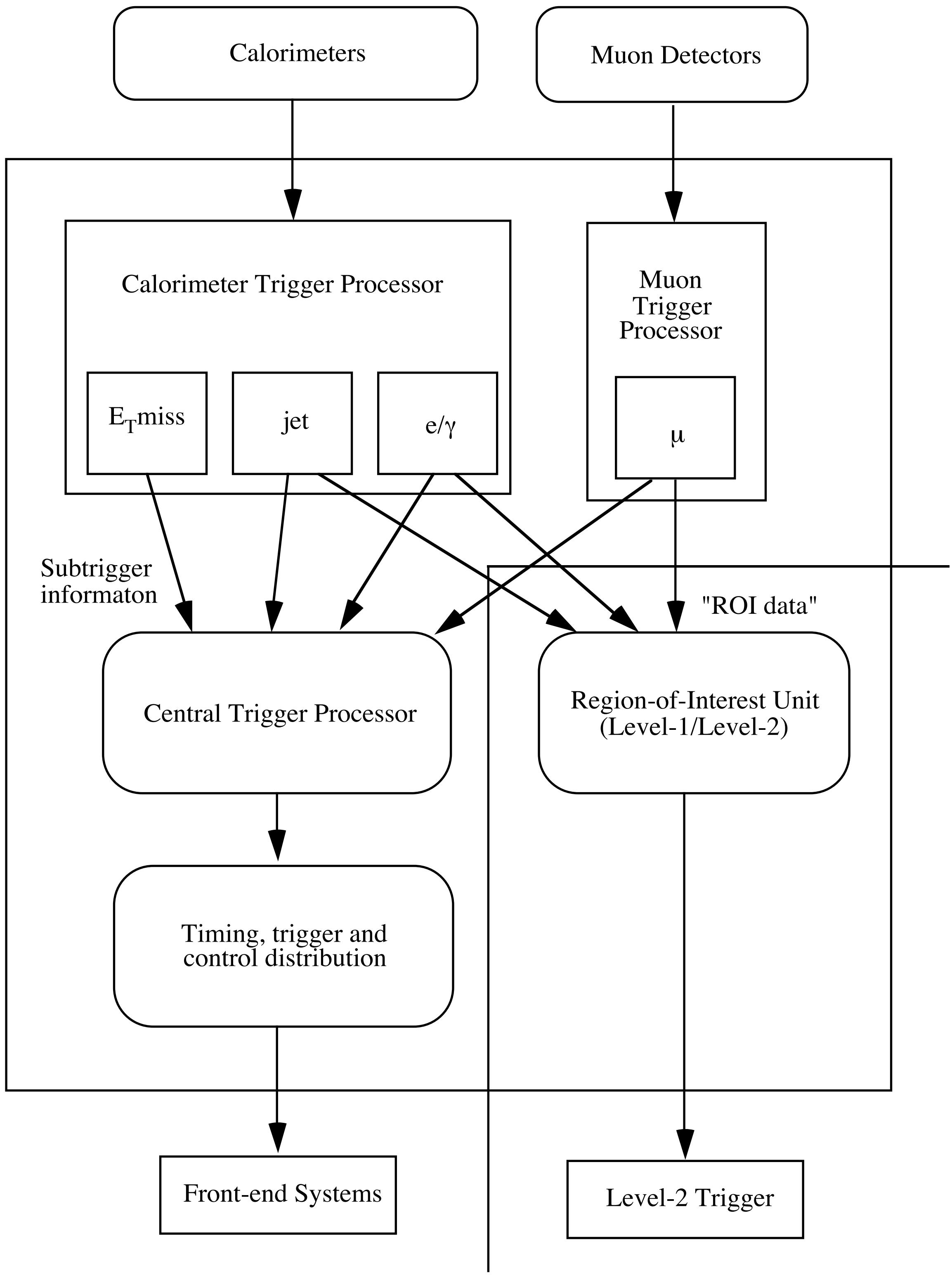
Rutherford Appleton Laboratory

Stockholm University

University of Wisconsin

First-level trigger — block diagram



In Feb 1995, approved for continuation:

Milestones for 1995

- Beam tests of a second-generation muon-trigger processor incorporating a coincidence-matrix ASIC.
- Beam tests of bunch-crossing identification logic for the calorimeter based on FPGAs, using a new FADC system.
- Evaluation of key components of the central trigger processor in gate arrays.
- Development of demonstrators for key components of calorimeter trigger processors including evaluation of:
  - fast optical links and integrated optics;
  - fast electrical data transmission between boards and crates;
  - fast high-density processing ASICs.
- Submission of a bit-serial demonstrator ASIC to a manufacturer.

Propose to continue for one more year

Areas where we consider that continued collaboration for one more year within RD27 will be valuable:

- High-speed, synchronous data links for transmitting data to trigger processors.
- High-speed custom backplanes for inter-module communication within trigger processors.
- Assessment of FPGAs as components for trigger processors, especially in the central trigger processor where the number of processing units required does not justify a custom circuit development.
- Evaluation of alternative ASIC technologies and designs.

All of the above are continuations of ongoing work.

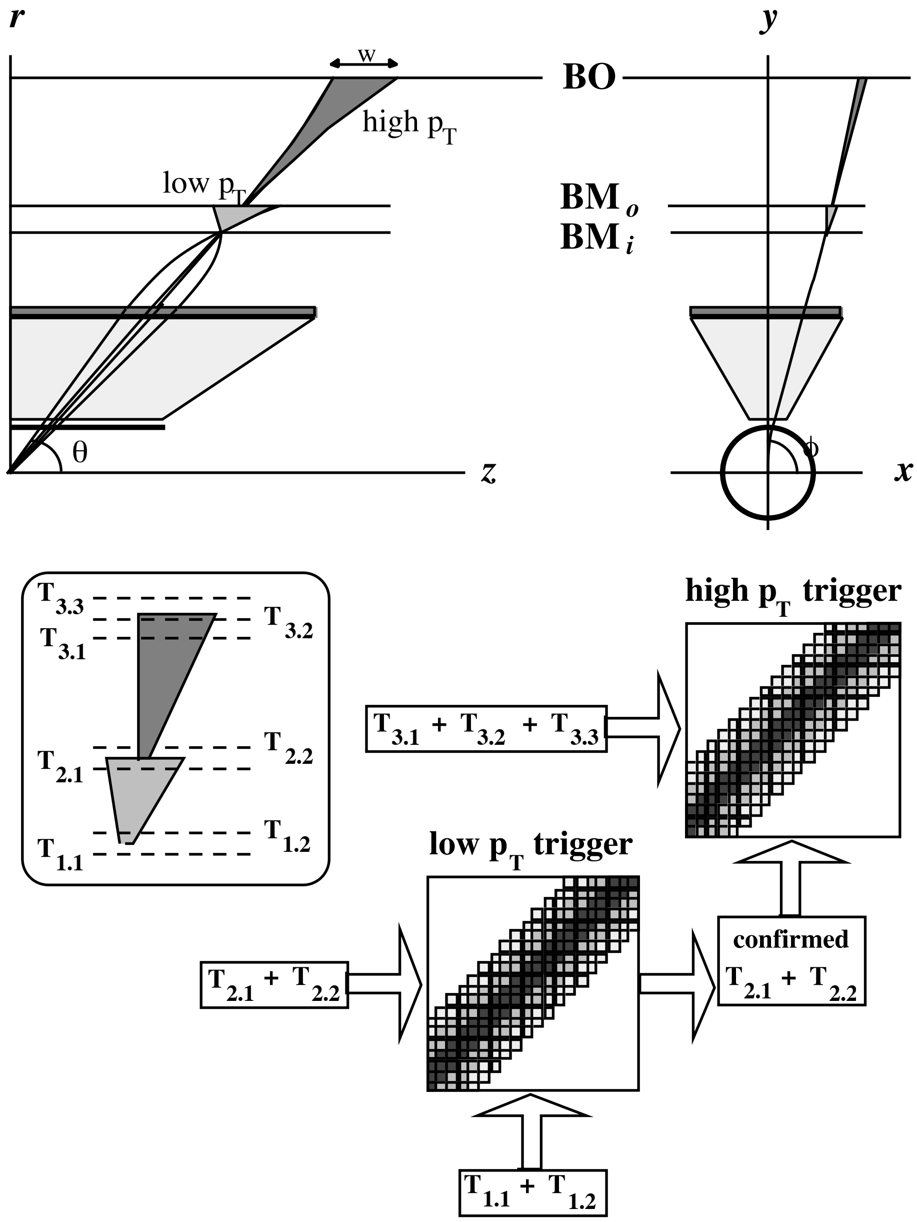
The results obtained will allow both ATLAS and CMS to benefit from a broader assessment of these items than would otherwise be possible.

Able to share specialist test facilities.

Promote use of common solutions within trigger systems.

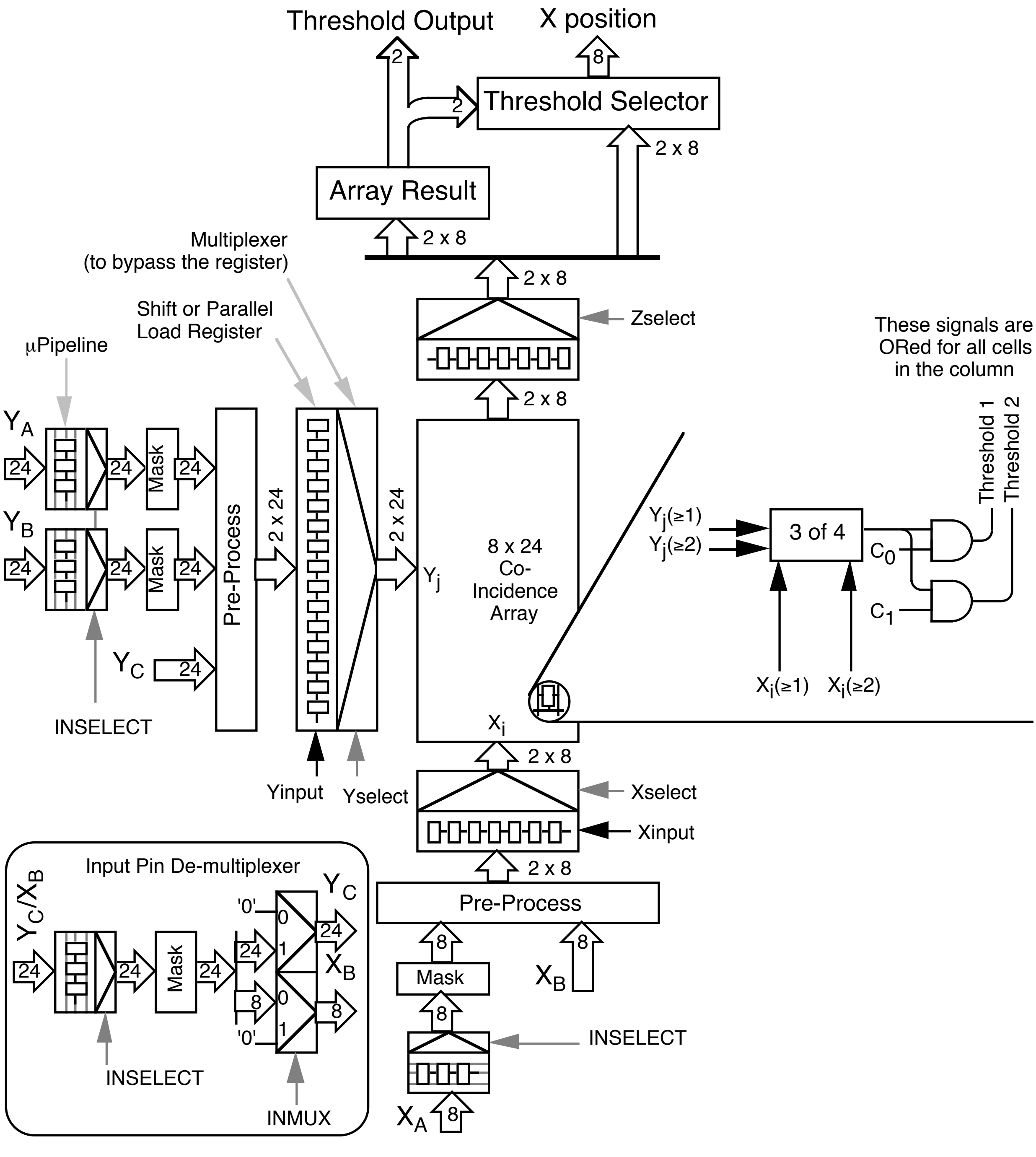
Muon Trigger

Muon-trigger algorithm (ATLAS)



Programmable coincidence matrix ASIC

- ASIC implemented in a 0.5 μm CMOS gate array from Fujitsu (34k gates).
- Measured maximum skew is 1.8 ns; device can operate at clock speeds up to 130 MHz.

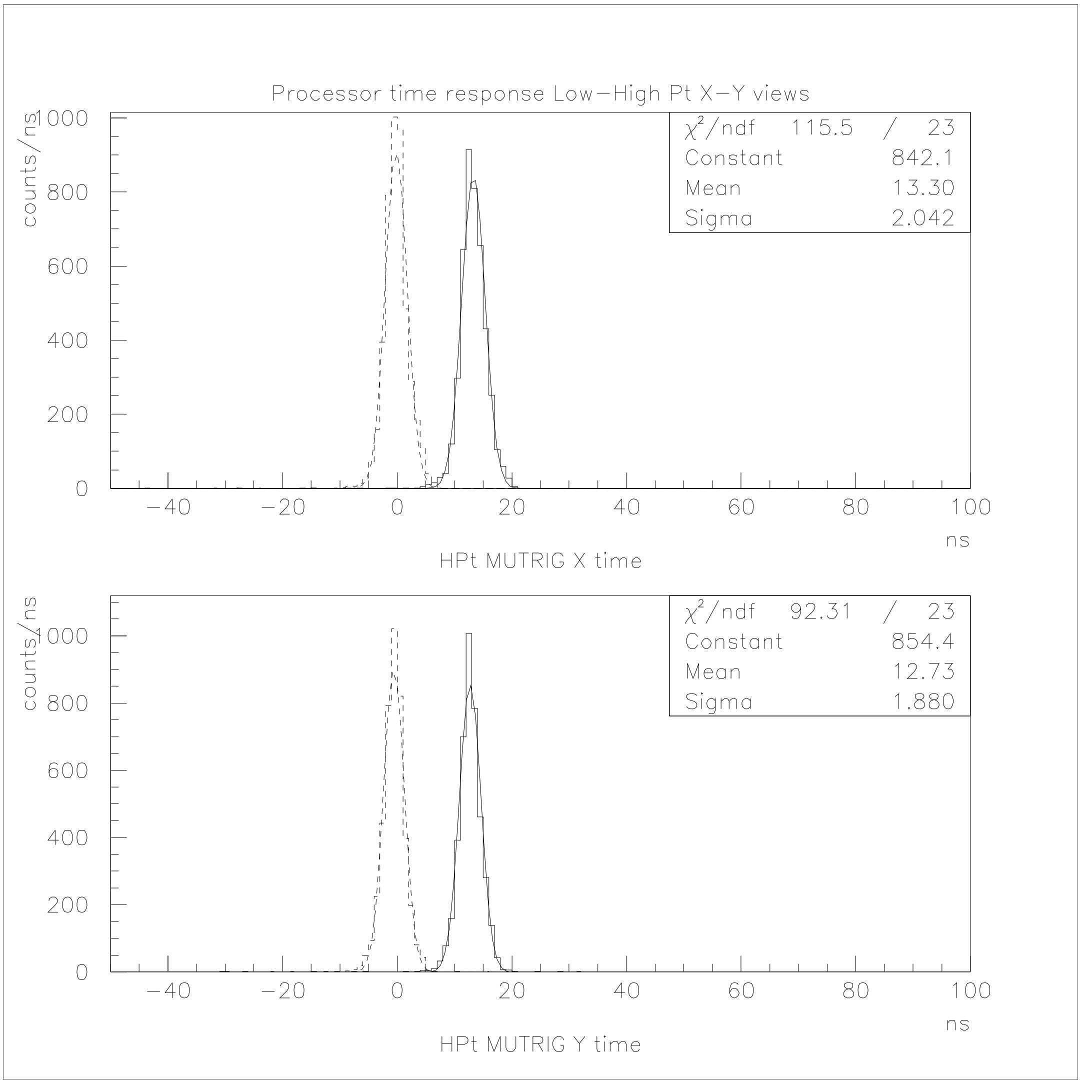


Block diagram of muon-trigger demonstrator ASIC.

Second-generation muon-trigger processor demonstrator

Beam tests at H8 test beam

The “trigger tower” measured about 50 cm by 50 cm, with seven layers per projection in a similar arrangement to the one planned for ATLAS.



Real-time performance of the demonstrator prototype.

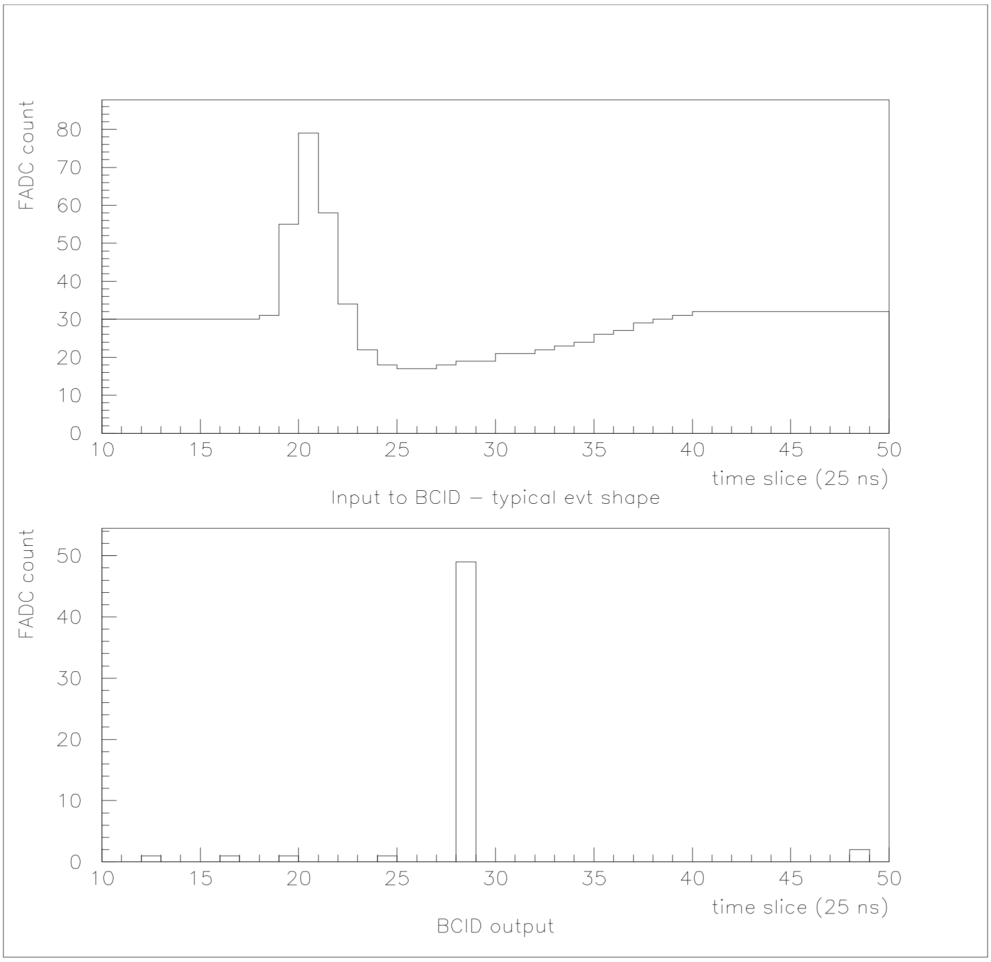
- Measured time resolution of trigger system ~ 2 ns.
- Latency for each of low- and high-p_T logic ~ 15 ns.

Continue work within ATLAS first-level trigger project.

Calorimeter Trigger

New FADC system

- VME modules containing four channels with 8-bit resolution.
- External clock input allows sampling rates of more than 80 MHz.
- Front-panel output of digitised data in real time.



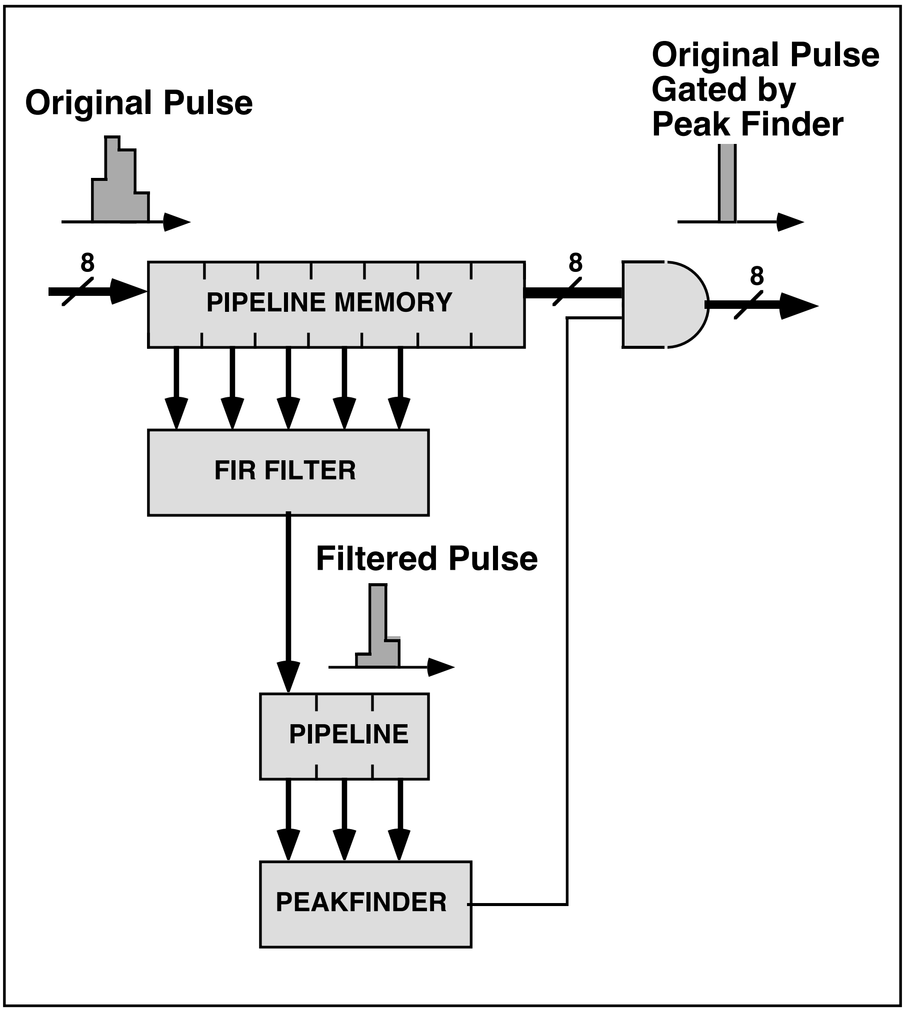
Example of calorimeter pulse recorded with the ADC system.

New FADC system used to test prototype trigger systems, sending the data over a differential-ECL crate-to-crate link.

So far, 12 modules built; 11 more to be made in 1996.

Bunch-crossing identification studies at the test beam

- Response time of LHC calorimeters longer than the 25 ns interval between bunch crossings.
- Necessary to perform bunch-crossing identification (BCID) processing.

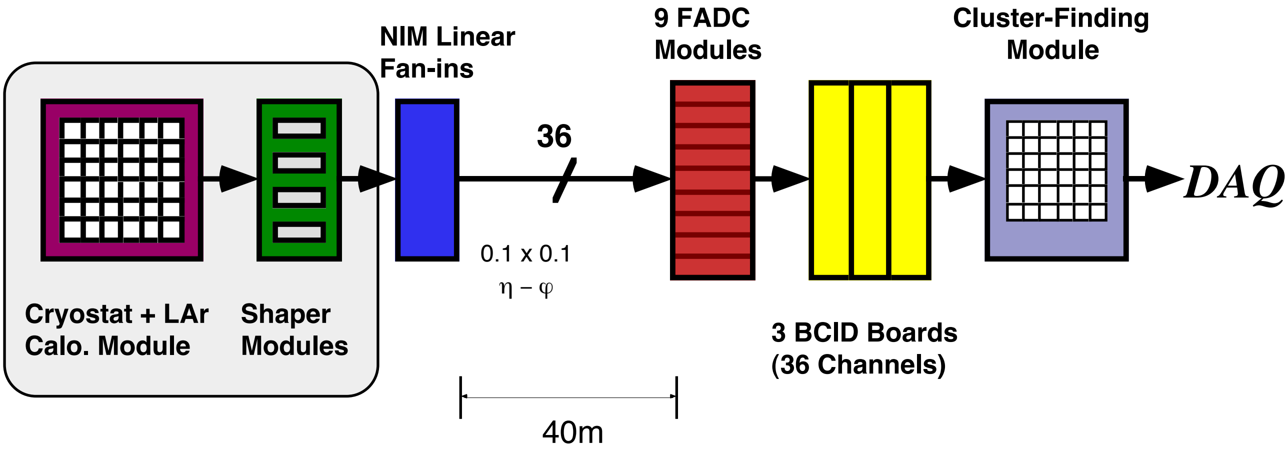


Block diagram of BCID logic.

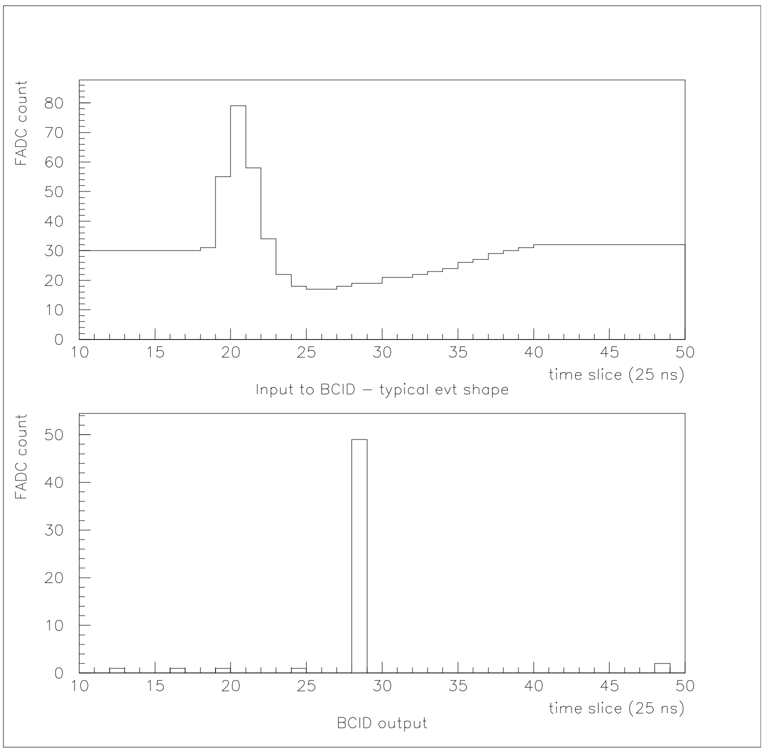
- Multi-channel demonstrator prototype based on FPGAs.
- Each 9U module handles 12□channels of 8-bit input data from the ADC system; each FPGA handles BCID processing for four channels.
- First ASIC implementation of a four-channel BCID processor has been implemented.

BCID results

Bunch-crossing identification has been successfully performed on calorimeter signals in real time using the FPGA system programmed with various algorithms, and using the ASICs.



Good efficiency is obtained for energies above about 2□GeV, which is adequate for triggering at LHC. Work is continuing to optimise algorithms for very small and very large pulses.



Studies of fast input data links

A major challenge for the calorimeter trigger processors of ATLAS and CMS is the data rate into these systems.

- With about 8000 8-bit words of input data per 25 ns period, the total data rate is 2560 Gb/s.
- Special requirements for the first-level trigger are synchronous links with fixed low latency.
- Both experiments assume ~ 1 Gb/s links each carrying data for two trigger cells
- Both experiments consider possibility of using HP G-link chipset.

A number of developments are in progress within RD27 related to the fast data links.

- Looking at the possible use of serial electrical links as an alternative to optical ones in case the digitisation system is placed in close proximity to the trigger processor.
- An evaluation is currently being made of optical links using the HP G-link chipset and Finisar optical transmitter/receiver modules.
  - Demonstrator modules designed at RAL for BaBar experiment modified to operate in simplex mode; preliminary tests made running the links at 75 MHz with 20-bit frames and at 80 MHz using 16-bit frames.
- An alternative to using the HP G-link chipset would be a custom solution making use of the availability of a common 40 MHz clock at the transmit and receive ends of the data links.

Commercial optical/electrical components and chipsets tend to be physically quite large. Our application is unusual in the requirement to bring tens or even hundreds of optical fibres onto individual circuit boards.

- Consider novel solutions such as integrated optics and multi-chip modules containing unpackaged components (e.g. unpackaged G-link circuits).
- During 1996, initial studies of the input data links will be made using a modular demonstrator system with discrete optical/electrical conversion and serial/parallel conversion components mounted on a daughter-board.
  - Provision made to include an MCM containing optical/electrical conversion and serial/parallel conversion at a later stage.

While we have not yet manufactured an integrated-optics MCM, detailed design studies have been made for a four-channel circuit, including extensive consultation with industry.

- Such circuits are feasible, and several companies have offered to build them for us.

In view of the common interest of the LHC experiments, it is proposed to continue this work during 1996 within the RD27 project.

Studies of high-speed backplanes

Studies are under way for high-speed custom backplanes for inter-module communication.

- Have designed 160 MHz backplanes based on differential-ECL and on BTL signal levels.
- BTL backplane has recently been manufactured, and it will be evaluated during 1996.
- ECL backplane will be built and evaluated during 1996.
- Investigating the possibility of a 320□MHz backplane based on LVDS differential signals.

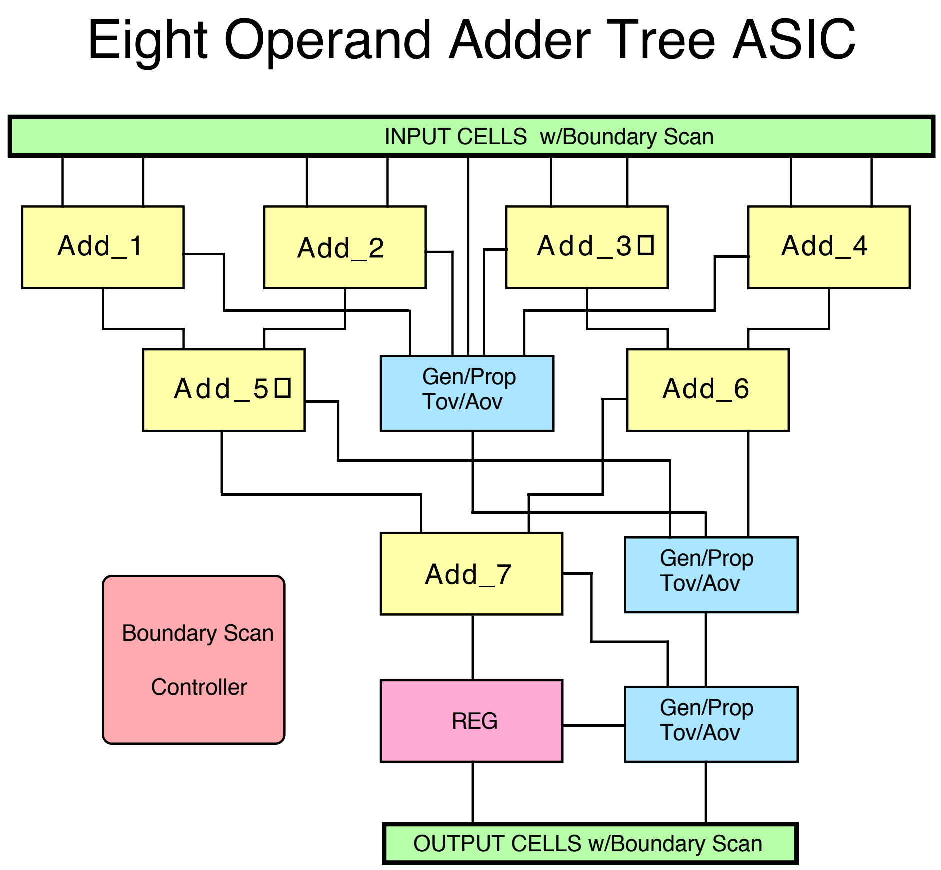
In view of the generic nature of the studies on high-speed custom backplanes, we propose to retain this work in the RD27 programme for 1996.

Development of fast, high-density processing ASICs

A number of ASIC developments related to calorimeter trigger processors have been made during the last year.

High-speed adder ASIC

- A very high-speed adder ASIC has been manufactured using a 0.6 μm GaAs process from Vitesse.
- ASIC has eight operands of 13 bits, consisting of 10 bits of value, sign, input-value and arithmetic overflow.
- Tested to 200 MHz (limited by available test facilities); simulation shows it should function at > 300 MHz.
- May test at higher speeds using facilities in Heidelberg.
- ASICs (and the design) available for ATLAS and CMS.

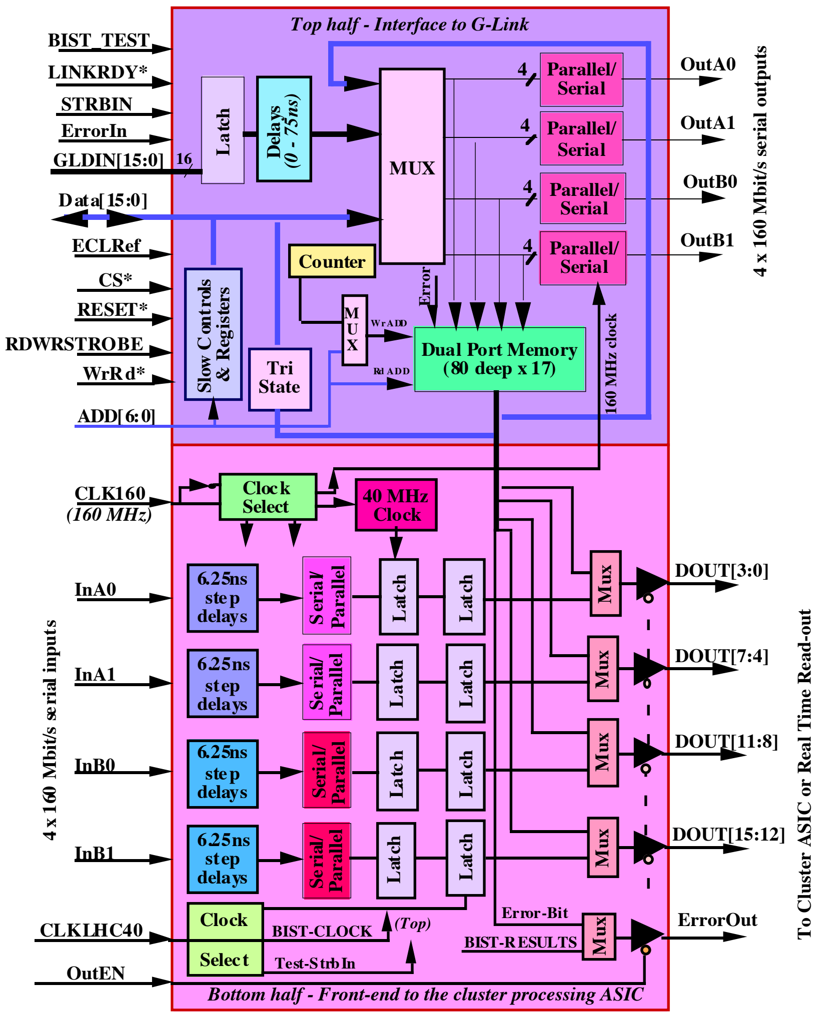


Block diagram of high-speed adder ASIC.

Dual-function multiplexer/demultiplexer ASIC

- Dual-function MUX/DEMUX ASIC designed and manufactured (ES2 0.7 µm CMOS).
- In first mode, it multiplexes 16 bits of data at 40 MHz into four bits of data at 160 MHz.
- In second mode, it performs the inverse operation.
- Reduce by a factor of four the number of connections between components, running at a speed four times higher than the bunch-crossing frequency.

Dual-function MUX/DeMUX ASIC

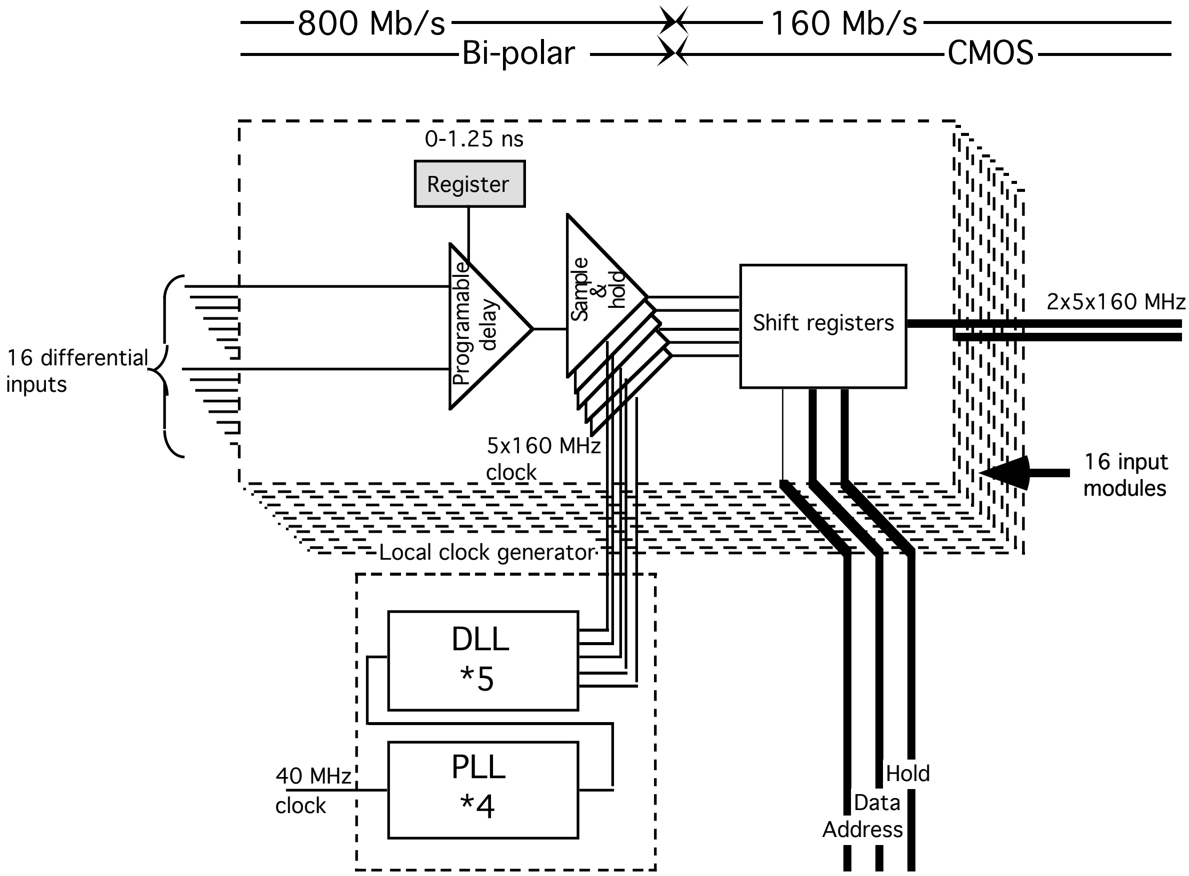


Dual-function ASIC block diagram.

Bit-serial test ASIC

A test ASIC for the 800 MHz input part of the bit-serial processor development has been designed and submitted for manufacture.

- Receive 16 serial inputs at 800 MHz, and perform serial-to-parallel conversion.
- The ASIC is being manufactured in a 0.6 μm BiCMOS process by Ericsson, and delivery is scheduled for February 1996.
- Testing of this ASIC will be performed in Stockholm and in Heidelberg.



Block diagram of the test ASIC

Bunch-crossing identification ASIC

- BCID ASIC was manufactured in a 1 μm process by ES2.
- Tested in the laboratory and then successfully integrated in the demonstrator system at the test beam.
- Plan to develop and manufacture a second-generation BCID ASIC that will include additional functions: look-up tables for calibrating the input data, pipelined readout with a derandomising buffer for deadtime-less operation, and a test facility consisting of "playback memory".

Central Trigger Processor

Design of a central trigger processor (CTP) demonstrator is well advanced.

- This demonstrator will contain all the essential elements of a final system, and will work at full speed with the required low latency (≤ 125 ns).
- Had originally envisaged using custom gate arrays for the CTP. Found that sufficiently large and fast FPGAs are now available to construct a compact system that can operate within the required low latency. A study has been performed of the feasibility of implementing the key components of the CTP in FPGAs.

The status of the system is that all of the FPGA parts have been designed and simulated.

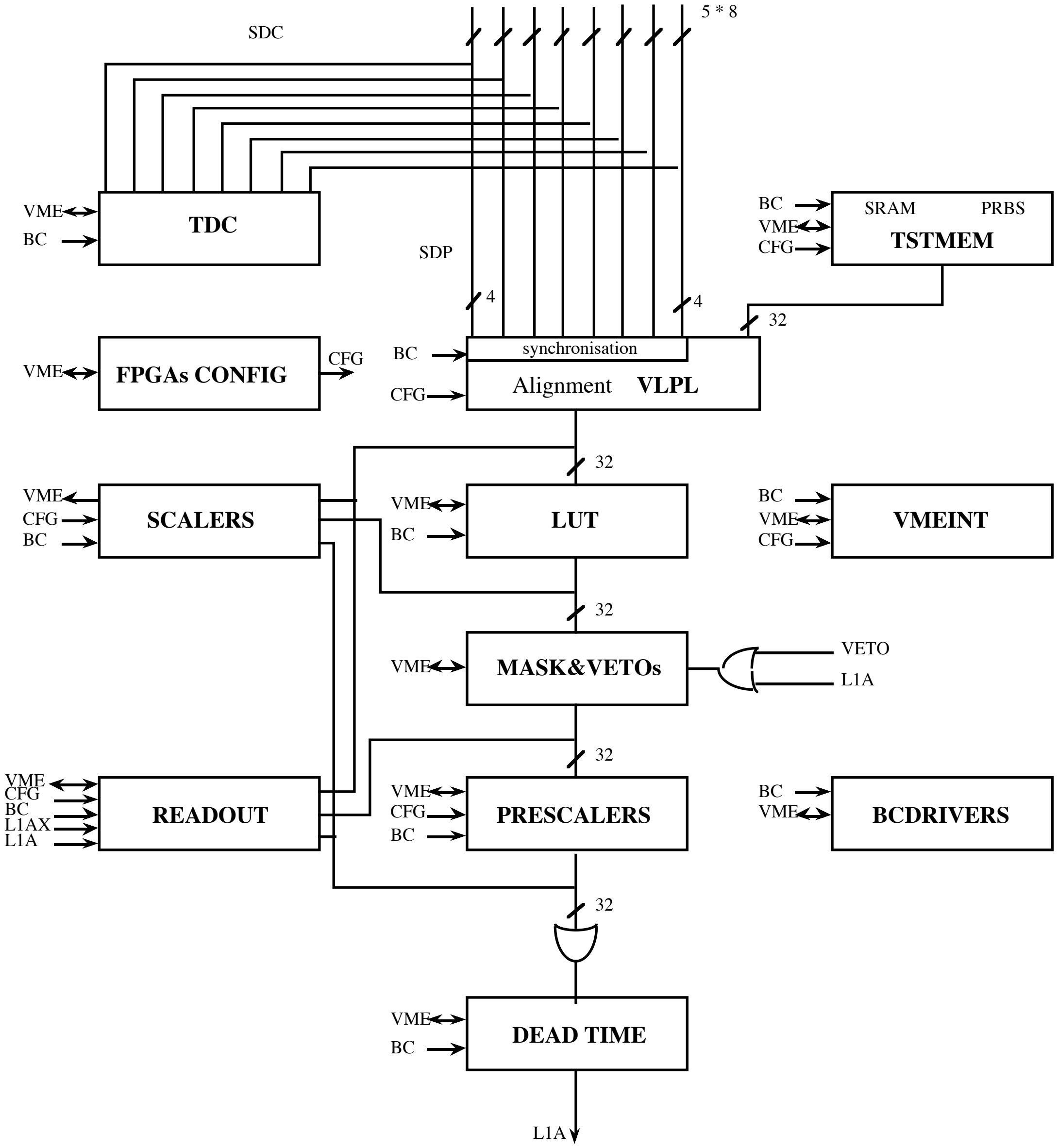
- The demonstrator will be implemented as a 9U VME module which will be tested in the laboratory and at the test beam during 1996.

The CTP development is of general interest to the LHC experiments, all of which will need components such as prescalers, scalers, etc. In contrast to the calorimeter and muon trigger processors, the CTP design does not depend strongly on the particiuliarities of the detectors. We therefore propose to continue the work on the CTP demonstrator within RD27 for a final year.

Components of the CTP

- Variable-length pipeline (VLPL) — alignment of the different groups of signals in time. Alignment of the 32 input signals will be performed in a single FPGA circuit, reconfigurable in situ to adjust the delays.
- “Look-up table” (LUT), performs the trigger algorithm which allows combinations of the inputs to be required in coincidence, veto or “don’t care”. It is implemented using a combination of SRAM and discrete logic.
- Mask and veto logic allows individual triggers to be masked, for example to introduce deadtime preferentially for low priority triggers, or for a global veto to be applied.
- Prescaler block allows the 32 triggers to be prescaled by independently programmable factors. Each FPGA will include 16 prescalers.
- Scalers monitor the rates at various points in the system — each FPGA contains 32 12-bit scalers with associated read-out registers.

Block diagram of CTP demonstrator



Conclusion

Propose continuation of RD27 for one more year

We suggest the following milestones for the final year of the project, focusing on items that are part of our ongoing programme and are of common interest across the LHC experiments:

- Tests of very high-speed (≥ 800 Mbit/s) synchronous serial data links for transmitting data to trigger processors.
- Tests of high-speed (≥ 160 Mbit/s) custom backplanes, based on BTL and differential-ECL signals, for communication between trigger-processor modules.
- Provision of demonstrator systems for central trigger processors based on FPGAs.

Request to CERN

The request to CERN relates to work on the central trigger processor :

- Boards and components for CTP demonstrator 30kCHF
- Computing equipment for CTP demonstrator 20kCHF
- Travel for RD27 meetings; stores 15kCHF

The 50kCHF request to CERN for investments in 1996, is to be compared with the total expected funding for RD27-related work of about 500 kCHF.

We request continued electronics-engineering support from ECP division at the same level as in 1995.